CHAPTER 7

CONCLUSIONS

This paper presents a new method for efficiently checking hazard-freedom in gate-level timed circuits. This method uses a cube approximation of the internal signal behavior in order to avoid generating an explicit state graph representing the switching behavior of the internal signals. Our experimental results show that this new method can be substantially faster than previous gate-level timing verification tools. While this method is conservative and thus can report some incorrect hazards, the number of such false negative results appears to be small. This method has been shown to scale very well in that it can verify examples with more than 80 gates in less than a second while previous methods fail to complete.

The long term goal of this work is to use this hazard analyzer to guide technology mapping of timed circuits. In asynchronous circuits, hazards must be avoided and care must be taken during technology mapping to not introduce hazards in the design. Therefore, an asynchronous technology mapper requires a method to rapidly determine when a transformation of the netlist has introduced a hazard. The hazard analyzer described in this paper addresses this need making efficient technology mapping of timed circuits possible.

7.1 Future Work

What about the idea of allowing wome hazards to exist in the synthesized equations before I even start decomposition? Would this indicate a bad synthesis or allow more flexibility to the whole process?

- Identify context and trigger signals for the cover under consideration and place these signals wisely in the decomposition [40].

- Examine the nature of transitions involved and use the work in [52] to determine a potentially hazard-free decomposition.
- Investigate state signal insertion methods described in [41] to create a hazard-free decomposition.
- Add wire acknowledgment forks described in [52] where necessary.
- Further investigate the work of Kondratyev in [28] and apply his methods, if possible, to timed circuits.