Chapter 12

Lecture 13

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Circuits

Automatic Test Generation for Combinational

\begin{align*}
\text{yield} \times \text{frac. of faults covered by a test} \\
\times \text{frac. of detected faults} = \text{frac. of faults detected} \\
\text{frac. of faults detected} = 1 - \text{frac. of undetected faults} \\
\text{frac. of undetected faults} = 1 - \text{frac. of detected faults}
\end{align*}

Introduction
Testing Methods

- Vertices in specific faults are present in the CNT.
- Knowledge of the structure of the CNT is essential.
- Based on assumed fault set.

Structured testing:

- Vertices CNT perform as expected.
- No assumptions about structure of circuit under test (CNT).
- Few assumptions about failure mechanisms and faults.

Functional testing:

A Short-Circuit (Stick-at-0 Fault)
Stuck-at Faults:

- Fault site:

Equivalent Faults:
Excitation and Sensitization

To sensitize a path, all side inputs must be non-controlling.

- XOR and XNOR gates do not.
- AND, OR, NAND, and NOR gates have controlling values.

Excitation and Sensitization
Multiple Tests Possible

A Redundant Combinational Circuit
Has Conflicts but Testable

Use of Compound Values
Frontier Element (G4) and Unfounded Element (G1)

Decision Trees

<table>
<thead>
<tr>
<th>a=b=1, f=0, e=0/1, g=1/0</th>
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<tbody>
<tr>
<td>0/1</td>
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Test

Conflict

c=1

1

p

0
Example of Implications

Another Example of Implications
Algorithm

1. Apply the fault extraction condition.
2. Perform the implications of the last assignment.
3. If the fault symptoms have reached a primary output:
   a. If justification fails, backtrack and go to step 2, else exit.
   b. Justify the remaining unjustified lines.
4. If the frontier is empty, backtrack and go to step 2.
5. If frontier consists of one gate only, perform resultime.
6. Choose one signal not reachable from fault site and assign to it.
7. Either 1 or 0. Create a node in the decision tree, and go to step 2.
ATPG Example

Decision Tree for Previous Example
PODEM algorithm: always select primary input using backtrace.

FN algorithm: select funnel points or head-nose.
- Select unassigned input to an unflushed gate.
- Select unassigned input to a frontier gate.

D-algorithm:

Choice of the Decision Variables

Example of Backtrace
Repeat until fault list is exhausted.

- Use fault simulator to identify which faults detected.
- If fault is untestable, discard it.
- Pick a fault from list and generate a test for it.
- Identify equivalent faults and select representative.
- Generate all possible faults.

Putting the Pieces Together

A Redundant Circuit
Irrudundant Version of Previous Circuit

A Circuit with Multiple Redundancies
Another Redundant Circuit

Previous Circuit with Redundancy Removed
Previous Circuit with a New Redundancy Removed

A 2-bit Carry-Skip Adder
Demonstrated how ATPG tools can detect redundancies.

- Described a ATPG algorithm.
- Discussed various fault models.

Summary
Circuit for Problem 2: a = 0, b = 1, c = 1, d = 1, e = 0, f = 1/0, g = 1/0, h = 1/0, k = 1/0, l = 1/0, m = 1/0, n = 1/0, o = 1/0, p = 1/0, q = 1/0, r = 1/0, s = 1/0, t = 1/0, u = 1/0, v = 1/0, w = 1/0, x = 1/0, y = 1/0, z = 1/0

Decision Tree for Problem 2
Circuit for Problem 3: $g = a - 0$

Decision Tree for Problem 3

unique sens.
Circuit for Problem 4: h s-a-1

Decision Tree for Problem 4

Unique sens.:

\[
\begin{align*}
\text{test} &= 0 \\
\text{b} &= 0/1, 1/0, 1/1, 0/0, 1/1, 0/1, 1/0
\end{align*}
\]
Circuit for Problem 5: $f = s - a - 1$

Decision Tree for Problem 5
Circuit for Problem 6: $h \equiv a - 0$

Decision Tree for Problem 6

$\begin{align*}
\text{Test} & : a = 0, d = 1, c = 1, m = 1, n = 0, u = 1, t = 1, h = 1, g = 1, k = 0, l = 1, \\end{align*}$
Circuit For Problem 7: \( f \) Input to \( G4 \) s-8-1

Circuit For Problem 8: c s-8-0