CS/EE 5740/6740:
Computer Aided Design of Digital Circuits

Chris J. Myers

Course description

Computer Aided Design (CAD) systems play a key role in the design of Very Large Scale Integrated (VLSI) circuits. This course presents the techniques used for the Computer Aided synthesis of integrated circuits. Topics include: two-level logic synthesis, models for sequential systems, synthesis and verification of finite state machines, multi-level logic synthesis, automatic test generation, and technology mapping.

Prerequisites

Students should have a familiarity with computer programming (CS 201-2), digital logic design (EE/CS 361), and algorithms and data structures (CS 354). Courses in computer organization (EE/CS 362,3,7) and integrated circuit design (EE/CS 542,3,4,5) are strongly recommended.

Textbook


Grading policy for CS/EE 5740

- Homework/quizzes 30 percent
- Two midterms 30 percent
- Final or Project 40 percent

Grading policy for CS/EE 6740

- Homework/quizzes 30 percent
- Two midterms 30 percent
- Project 20 percent
- Final 20 percent
# Course Info

**COURSE:** CS/EE 5740/6740  
**Credits:** 3  
**Place:** EMCB 102  
**Time:** TTh 11:50am-1:10pm  
**Class email:** ee5740@ee.utah.edu  
**Class webpage:** http://www.async.elen.utah.edu/~myers/ee5740.html

**INSTRUCTOR:** Chris J. Myers  
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**Location:** MEB 4140  
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**Office Hours:** TTh 10:30-11:45am and by appointment
Tentative syllabus

1. Introduction
   - Motivation for CAD for VLSI
   - Overview of optimal logic synthesis
   - Graph algorithms and complexity
   - A quick tour of logic synthesis

2. Two-level logic synthesis
   - Boolean algebra
   - Synthesis of two-level circuits
   - Heuristic minimization of two-level circuits
   - Binary decision diagrams (BDDs)

3. Sequential logic synthesis and verification
   - Models of sequential systems
   - Synthesis and verification of finite state machines
   - Finite automata

4. Multilevel logic synthesis
   - Multi-level logic synthesis
   - Multi-level minimization
   - Automatic test generation for combinational circuits
   - Technology mapping