CS/EE 3710: Computer Design Laboratory

Chris J. Myers

Course description

This course applies knowledge of digital logic and computer architecture to the design and implementation of a microprocessor. Students will be given benchmark programs and asked to design a microprocessor which will execute them efficiently. Students are taught the VHDL hardware description language as a way to specify and simulate alternative architectures for their microprocessor. From the final VHDL specification, an FPGA implementation will be synthesized.

Prerequisites

Students should have a familiarity with computer programming (CS 2010-2020), digital logic design (EE/CS 3700), and computer architecture (EE/CS 3810).

Textbooks

For this course, you will need a book on VHDL. I will be roughly following the VHDL Starter’s Guide by Sudhaker Yalamanchili. For someone who plans to use VHDL professionally, I recommend Peter Ashenden’s The Designer's Guide to VHDL. You are free to use any VHDL book which looks appropriate for you. I have several in my office, if you would like to check them out.

Project

The majority of this class will be spent designing and implementing a microprocessor in a team of two. You will be given 3 benchmark codes in C. Your job will be to design an instruction set, determine a microprocessor architecture, simulate and test using VHDL, and implement in FPGAs. The three best projects in terms of cost/performance will win prizes.

Grading policy

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<td>Labs</td>
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Course Info

Course: CS/EE 3710
Credits: 3
Place: EMCB 105
Time: TTh 9:10-10:30
Class webpage: http://www.async.elec.utah.edu/~myers/ee3710

Instructor: Chris J. Myers
Electronic Mail: myers@ee.utah.edu
Location: MEB 4140
Telephone: (801) 581-6490
Office Hours: TTh 10:30-noon

Teaching Assistant: Ron Lenk
Electronic Mail: lenk@eng.utah.edu
Location: EMCB 210
Office Hours: MW 8-10:30am, 2-4:30pm
Office Hours: TTh 1-3:30pm
TENTATIVE syllabus

1. Lectures:
   - 8/26 - Introduction to VHDL and simulation (Chapters 1, 2, and 3)
   - 8/31 - Introduction to VHDL, cont. (Chapter 3)
   - 9/2 - Modeling behavior (Chapter 4)
   - 9/7 - Modeling behavior, cont. (Chapter 4)
   - 9/9 - Modeling structure, (Chapter 5)
   - 9/14 - Subprograms, packages, and libraries (Chapter 6)
   - 9/16 - Basic Input/Output, (Chapter 7)

2. Labs:
   - 9/2 - Lab 1 due: VHDL simulation using Veribest
   - 9/9 - Lab 2 due: behavioral VHDL
   - 9/16 - Lab 3 due: structural VHDL and packages
   - 9/23 - Lab 4 due: VHDL I/O and testbenches

3. Project milestones:
   - 9/2 - Project milestone 1: select partner
   - 9/21, 9/23 - Project milestone 2: ISA designed
   - 9/28, 9/30 - Project milestone 3: Write assembler for ISA
   - 10/5, 10/7 - Project milestone 4: VHDL behavioral model of ISA
   - 10/12, 10/14 - Project milestone 5: Block level design of datapath
   - 10/19, 10/21 - Project milestone 6: VHDL behavioral model of datapath
   - 10/26, 10/28 - Project milestone 7: FSM controller design
   - 11/2, 11/4 - Project milestone 8: VHDL behavioral model of the FSM
   - 11/9, 11/11 - Project milestone 9: Complete logic synthesis
   - 11/16, 11/18 - Project milestone 10: Complete schematics for hardware
   - 11/23 - Joint lab session with brief project reports
   - 11/30, 12/2 - Project milestone 11: Complete hardware design
   - 12/7, 12/9 - Project demonstrations
   - 12/15 - Project report due