CS/EE 3710: Computer Design Laboratory

Chris J. Myers

Course description

This course applies knowledge of digital logic and computer architecture to the design and implementation of a microprocessor. Students will be given benchmark programs and asked to design a microprocessor which will execute them efficiently. Students will design their microprocessor using a combination of VHDL and schematics. From the final VHDL specification, an FPGA implementation will be synthesized.

Prerequisites

Students should have a familiarity with computer programming (CS 2010-2020), digital logic design with VHDL (EE/CS 3700), and computer architecture (EE/CS 3810).

Textbooks

For this course, you will need a good VHDL reference. I have selected Introductory VHDL From Simulation to Synthesis by Sudhaker Yalamanchili. This book also comes with a student edition of Xilinx’s Foundation software which may be useful to you, if you like to work from home. For someone who plans to use VHDL professionally, I also recommend Peter Ashenden’s The Designer’s Guide to VHDL.

Grading policy

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<th>Component</th>
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<tr>
<td>Milestones</td>
<td>30 percent</td>
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<td>Oral Reports</td>
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Course Info

COURSE: CS/EE 3710  
Credits: 3  
Place: EMCB 105  
Time: TTh 9:10-10:30  
Class webpage: http://www.async.ece.utah.edu/~myers/ee3710

INSTRUCTOR: Chris J. Myers  
Electronic Mail: myers@vlsigroup.ece.utah.edu  
Location: EMCB 210  
Telephone: (801) 581-6490  
Project Meetings/Office Hours: TTh 9:10-11:30

TEACHING ASSISTANT: James Bergstrom  
Electronic Mail: bergstro@eng.utah.edu  
Location: EMCB 210  
Project Meetings/Office Hours: MTWTh 1-5pm
Project

During this class you will design and implement a microprocessor in a team of three. Note that grades will still be given individually, not just to the team. You will be given 3 benchmark codes in C. Your job will be to design an instruction set, determine a microprocessor architecture, simulate and test using VHDL, and implement in FPGAs. The better your design performs, the better your grade. Therefore, you should consider advanced architecture features such as pipelining, branch prediction, hardware multipliers, etc.

The implementation technology is boards from Xess that feature a Xilinx FPGA, on-board SRAM, and some other goodies. Currently, we have 5 Xess 4010XL boards in the DSL lab which include 7k to 20k gates and 128KByte SRAM. We are ordering several Xess XSA-100 boards which include a Spartan2 Xilinx chip with 100,000 gates and 16MBytes SDRAM.

All projects will be designed with VHDL and/or schematics and simulated/synthesized using CAD tools (some info is on the website). You have a choice of several tools:

- Mentor’s FPGA Advantage (NT lab):
  - PROS: supports VHDL simulation and synthesis.
  - CONs: does not support schematic capture.

- Mentor’s DesignView (NT lab):
  - PROS: supports both VHDL and schematics.
  - CONs: had some problems when used in 3710 before.

- Xilinx Foundation (NT lab, student edition with your book):
  - PROS: supports VHDL/schematic design, can use at home.
  - CONs: does not supports direct VHDL simulation.

- Viewlogic’s PowerView (CADE lab):
  - PROS: familiar with it from CS/EE 3700,
  - CONs: there were many problems with it in CS/EE 3700.

Most of the time we will be meeting in project group meetings in our class time slot to follow your group’s progress and to give advice. We will check off your milestones during our meeting time. Project groups will meet either with Myers (TTh 9:10-11:30) or Bergstrom (MW 1-3:20) each week in EMCB 210. We will meet on October 2nd and November 20th as a group at the class time for oral project reports. In the first, you will present your ISA to the class. In the second, you will present your architecture.

The project will include several milestones. Whether your final project works or not, you will receive a lower grade if you fail to meet your milestones. You must also present your project both orally and in a final written report.
Project Milestones

- 8/24 - Project milestone 1: select partner(s) and meeting time.
- 9/3-9/6 - Project milestone 2: ISA designed (benchmarks compiled).
- 9/10-9/13 - Project milestone 3: Write assembler for ISA.
- 9/24-9/27 - Project milestone 4: VHDL behavioral model of ISA.
- 10/2 - MEET IN CLASS: Oral project report 1
- 10/15-10/18 - Project milestone 5: Complete datapath design.
- 10/29-11/1 - Project milestone 6: Complete VHDL design of FSM.
- 11/8-11/11 - Project milestone 7: Complete logic synthesis, begin testing hardware.
- 11/20 - MEET IN CLASS: Oral project report 2
- 12/3-12/6 - Project demonstrations (report due at demo).