LAB #1: Schematic Entry and Logic Simulation

This lab is due at 5pm in the EE locker for CS/EE 3700 on Thursday, January 21, 1997
NO LATE HOMEWORK WILL BE ACCEPTED.

1 Objectives

In this laboratory, you will learn how to use a schematic capture system to draw the network of logic gates that constitute your design. The major advantage of computer-based capture of your design is that the computer can simulate the logical behavior of your design. This allows you to verify that the circuit operates as you expect it to, even before you build it in the laboratory. Thus, the laboratory also introduces you to a simple logic simulator that allows you to look at logic 1's and 0's attached to nodes within your schematic.

2 Prelaboratory Exercises

You should be familiar with the function of basic AND and OR gates. Study your text to learn about the behavior of the half-adder and full-adder circuits. The following exercises should be completed on the attached Summary Sheet before you do the laboratory.

1. The half adder is a function that takes two inputs, X and Y, and produces two outputs, SUM and CARRY. Fill in the truth table for the behavior of the half-adder on the lab summary sheet. Draw a schematic for the half adder as well. You may use only NOT (INVerters), AND, and OR gates.

2. The full adder is a generation of the half adder that takes three inputs, X, Y, and CARRY-IN, and produces three outputs, SUM and CARRY-OUT. Fill in the truth table for the behavior of the full adder on the summary sheet. Draw a schematic for the full adder in the space provided on the summary sheet. Once again, you may only use NOT (INVerters), AND, and OR gates.

3. You can build a full adder using half adders and logic gates. Draw a schematic for a full adder built in this way in the space provided on the summary sheet.

3 Starting DesignView

DesignView is a comprehensive CAD system for entering gate level schematics of a digital system and performing simulations of its logical behavior. DesignView is executed by clicking on the VeriBest DesignView icon. The initial DesignView window is composed of 4 parts. The top part consists of pulldown menus and buttons to execute commands. If you move the mouse over the buttons, it will tell you what the command is that it executes. The left part is used to help you keep track of the design files in your current project. The bottom part is used to display messages from commands that you execute. The right side is your design capture window where you draw your schematics and stimulus waveforms.
4 Creating a new project

For each new design you do, you will want to create a project to organize your design files within. To do this, select from the menus: project → new. This opens a window and asks you for a project name and project location. For the project name, type lab1. For the project location, click on the ... button to the right and find the directory under your home directory in which you wish to place this project. Then, press Next. Then, it asks you to select a vendor technology, and you should select XilinxM1 XC3000 Technology and press Next. Then, it asks if you would like to add any design files. This option allows you to copy design files from an old project into this new project. This time, simply skip this step by pressing Next. The project is now created, so press Finish if everything is correct. You may get an error message saying that place and route tools are missing. You can ignore this error message, and simply press ok.

5 Schematic entry for the half adder

You are now ready to create the schematic for your half adder circuit. To create a new schematic, select from the menus File → New, and when prompted choose Schematic and press ok. You will now see a blank schematic in the right window. Your window maps onto a B-sized drawing: 17" by 11". So things are going to look fairly small when you draw them. Press the “magnifying glass” with a plus in it icon to zoom in at least until a positioning grid appears in the window (about 5 clicks). Now you are ready to start drawing a schematic!

Enter your schematic for the half adder based on your drawing for the prelab. Select the command: Place → Symbol. This command brings up a symbol menu. Double click on logic_3, and you should see a list of logic gate names. Next, you should choose a gate, such as AND2;1 (i.e., an AND gate with 2 inputs and 1 output) from the list by clicking on it. The symbol for the gate should then appear in the bottom window. If this is the gate you want, then click on place and move your mouse back to over your schematic window. Now, if you press the left button it will drop a instance of the gate you selected onto your schematic. If you need two gates, simply move your mouse to another location and select the left button again. Once, you have enough copies of the gate in your schematic, press the right button. This pulls up a small menu from which you should select cancel. Repeat the previous steps to grab all the gates that you need to build your half adder.

If you generate an extra gate by mistake, you can simply place your mouse over the gate and click on the left button. This will select the gate and turn it white. If you press the Delete key, it will delete the gate.

Next, we need to wire up the gates by adding wires (or nets) to the schematic. Select the command: Place → Wire. Now, move your mouse to where you would like the wire to start and click your left button once. This starts your wire, and subsequent single clicks can be used to make turns in your wire. Once you have routed your wire to its destination, double click the left button to stop the wire. If after routing a wire, you see a red dot on one end, this means the wire is floating or unconnected. If you were wiring two gates together, you can simply start a wire from the red dot to the gate you had intended to wire to. Use the previous steps to wire your gates together.

For inputs and outputs to your half adder, you need to use a slightly different procedure. For an input, again select the command: Place → Wire. However, before routing your wire, press the right button. This pulls up a menu from which you should select Add input hierarchical connector. This creates a wire which has an input pin on one end. Now route your wire to the input of the proper gate. For subsequent, connections to this input pin, you simply follow the instructions for wiring between gates and start the wire from the original wire. For an output, do the same as above except select Add output hierarchical connector instead.

You may have noticed that just above the schematic there are buttons with pictures of gates and wires. You can use these buttons to avoid using the pulldown menus to place gates and wires.
To make the inputs and outputs available for simulation purposes, you need to label them. To label an input or output port, you must select the point at which the hierarchical connector and the wire meet. To do this, click on the button labeled with a white area to go into select mode. Next, move the mouse over the point where the connector and wire meet and click on the left button. This point should turn white. Now, with your mouse over the white point, press the right button and select properties from the popup menu. In the properties menu, select the text tab and click in a blank area under the type field. This should produce a pulldown menu. From the pulldown menu, select Hier Pin Name. Next, click in the value field, and type the name you would like to give this input or output.

Once you have completed wiring up your half adder and all the inputs and outputs are labeled, it is a good idea to save your work. Select the following commands to do this: File → save, type the name of your schematic (i.e., HA), and click on save.

Before moving on to simulation, it is also a good idea to check that your schematic has no obvious errors. This can be done by selecting the command: Tools → Verify. This brings up a window to select what to verify. Simply, press ok. In the bottom part of the window, it will describe any problems with the schematic. If it says there are 0 errors and 0 warnings, then you are all set. Otherwise, it will tell you what problems were found and give you grid locations to locate the problems with.

To print out your schematic, select the command: File → Print Setup and change the orientation to landscape. Next, select the command File → Print, select a printer, and press ok.

6 Simulating your half adder

In order to simulate your half adder, you need to first create a stimulus waveform. After you saved your schematic, the design name should have appeared in the left part of the window. Move the mouse over this name, and press the right button to bring up a menu. From this menu, select Generate Stimulus. This will bring up a window with each of the inputs listed to the left and a time scale to the right. Move your mouse to the right side and push the right button and select edge insert. This allows you to now add an edge in the stimulus waveform. If the input waveform is at the bottom, it represents a logic 0 and if it is near the top it represents a logic 1. To change value, you use edge insert to create a rising or falling transition. You can also grab the waveform and move it up to 1 and down to 0. Draw input waveforms sufficient to fully test your half adder. When you are done, select File → Save and press ok.

You can create multiple stimulus files for a given design, so it is necessary to associate one with the design before you can simulate the design. To do so, again move your mouse over the name of your design in the left side of the window, press the right button, and select Associate Stimulus. You should see a window pop up which includes the file name: HA_stim.vhd, select this, and press ok.

Now, you are ready to simulate your half adder. To start up the simulator, move you mouse over the symbol HA in the left window, press the right button again, and select Open in Simulator. First, you need to compile your design, which you can do by selecting Workspace → Compile All. Next, you should select Workspace → Execute Simulator to start the simulator. Select the command Tools → New Waveform Window to create a waveform window in which to watch the simulation results. Move your mouse over the buttons in the waveform viewer, and click on the one labeled Add Signals. This brings up a window and allows you to select which signals you would like to watch. Click on the Add All button to watch all signals, and then click on the Close button. To simulate, select the command Simulate → Run. To print the waveform, select the command File → Print.

You can return to the schematic view by closing the simulation window. Select the command: File → Exit.
7 Creating a symbol

Now, we will create a symbol to stand for the half adder in other higher level schematics, such as the full adder. A symbol consists of a schematic shape and pins that represent connections to the outside world. You have already been working with symbols for AND gates, OR gates, and INVerters. Now you will be creating your own symbol for the HA. It can be used in other schematics just like the predefined symbols for the basic gates.

To create a symbol, move your mouse to the left side over the name of your schematic, press the right button, and select Create Block Symbol. This will bring up a schematic showing you the symbol you just created. You should save your symbol by selecting File → Save.

8 Building a hierarchical schematic: the full adder

We are now ready to create the full adder schematic using two instances of the half adder and an OR gate. Just as in the half adder, we begin by creating a schematic window. Select the command File → New, and when prompted choose Schematic and press ok. Again, zoom in until you see the grid. Use the command Place → Block and enter the name HA. You can now place the block as you did before for the various logic gates. Don't forget to save your work to disk and print out your top level schematic. Attach the print out to your lab summary sheet.

Follow the same process you did for the HA to simulate the FA. If when you put your mouse over “FA” and press the right button, Generate Stimulus is not highlighted, then press Set as Root. You should then be able to create a stimulus file. Be sure to step the simulation through all eight possible input combinations. Do you see any glitches on the waveforms? Where? How wide are they? Exit DesignView by selecting File → Exit.

9 Laboratory Summary

In this laboratory, we have seen how to enter schematics, create symbols, and use a logic simulator to verify the behavior of a logic circuit. This is just the beginning of your exposure to CAD tools. You will be using DesignView throughout the semester to design and simulate circuits before actually constructing them in the laboratory.
10 Summary Sheet

Name:
Lab Section:
TA:

1. The **Half Adder** (15 pts).

   (a) Fill in the Half Adder Truth Table:

   \[
   \begin{array}{c|c|c|c}
   X & Y & \text{SUM} & \text{CARRY} \\
   \hline
   & & & \\
   \end{array}
   \]

   (b) Draw the schematic of the half adder circuit, using only AND, OR, and NOT gates.
2. The Full Adder (25 pts).

(a) Fill in the Full Adder Truth Table:

\[
\begin{array}{cccc}
X & Y & \text{Carry-In} & \text{SUM} & \text{Carry-Out} \\
\end{array}
\]

(b) Draw a schematic that implements this function directly, using only AND, OR, and NOT gates:
(c) Draw another schematic, this time expressing the full adder in terms of wired together half-adders and any other logic gates you may need:
3. **Using DesignView to Capture and Simulate the Half Adder (40 pts).**

   (a) Print out your schematic and attach it to this laboratory write up.

   (b) Attach a plot of your waveform to the summary. Annotate it with a description of the events that you see. Did you see anything unexpected during simulation? Explain what you see:
4. The Full Adder (20 pts).

(a) Attach a print out of the full adder schematic to the summary sheet.
(b) Attach annotated waveform plots. Do you see anything unusual in your output waveforms? If so, how do you explain it?