CS/EE 3700: Fundamentals of Digital System Design

Chris J. Myers

Course description

This course teaches the fundamental theory and design methods for digital systems. Topics include: logic functions minimization, combinational circuit design, synchronous and asynchronous sequential circuit design, state diagrams, Mealy and Moore circuits, state minimization and assignment, basic computer organization, and controller implementation. This course also teaches the use of software tools for design, minimization, simulation, and schematic capture of digital systems. The digital systems that are designed will be implemented using MSI, LSI, and field programmable gate arrays.

Prerequisites

Computer programming (CS 2010) and PHYCS 2220.

Textbook


Grading policy

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<tr>
<th>Component</th>
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<tr>
<td>Labs</td>
<td>30 percent</td>
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<tr>
<td>Midterms</td>
<td>30 percent</td>
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<tr>
<td>Project</td>
<td>20 percent</td>
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<td>Final</td>
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Discussion sections

The discussion section will be held in MEB 3133 (digital lab). You are required to signup for a discussion section.

1. Monday 8:35-9:25 (Eric Mercer)
2. Monday 2:00-2:50 (Glenn Miles)
3. Tuesday 7:30-8:20 (Eric Mercer)
4. Tuesday 12:55-1:45 (Kip Killpack)
5. Tuesday 2:00-2:50 (Eric Mercer)
6. Wednesday 10:45-11:35 (Ryan Hayward)
7. Wednesday 4:10-5:00 (Shiv Sompur)
8. Thursday 2:00-2:50 (Ryan Hayward)
9. Thursday 3:05-3:55 (Kip Killpack)
10. Friday 9:40-10:30 (Shiv Sompur)
11. Friday 12:55-1:45 (Glenn Miles)

TA office hours

The TA office hours will be held in EMCB 210 (NT lab).

1. Monday 9:00-12:00 (Shiv Sompur)
2. Monday 2:00-5:00 (Kip Killpack)
3. Tuesday 2:00-5:00 (Ryan Hayward)
4. Wednesday 8:00-10:00 (Eric Mercer)
5. Wednesday 10:00-1:00 (Shiv Sompur)
6. Wednesday 1:00-4:00 (Glenn Miles)
7. Wednesday 3:30-6:30 (Ryan Hayward)
8. Thursday 11:00-2:00 (Glenn Miles)
9. Thursday 3:00-5:00 (Eric Mercer)
10. Friday 12:00-3:00 (Kip Killpack)
Course Info

Course:
Credits: CS/EE 3700
Place: 4
Time: EMCB 101
Class newsgroup: TTh 8:35-10:30
Class webpage: uu.cs.class.3700
http://www.async.elec.utah.edu/~ee3700

Instructor:
Electronic Mail: Chris J. Myers
Location: myers@ee.utah.edu
Telephone: MEB 4140
Office Hours: (801) 581-6490
TTh 10:45-11:45

Head TA:
Electronic Mail: Eric Mercer
ee.mercer@ee.utah.edu

TA:
Electronic Mail: Ryan Hayward
rhayward@cs.utah.edu

TA:
Electronic Mail: Kip Killpack
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TA:
Electronic Mail: Glenn Miles
miles@eng.utah.edu

TA:
Electronic Mail: Shivakumar Sompur
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TA:
Electronic Mail: A.J. Palmer
apalmer@eng.utah.edu
Extended TENTATIVE syllabus

• Section 1: Combinational logic design (weeks 1-5)
  
  – Lecture topics:
    * Introduction to digital system design
    * Logic functions, switches, and gate logic
    * Two-level simplification
    * CAD Tools for simplification
    * Multilevel logic synthesis
    * Hazards and glitches and how to avoid them
    * Programmable arrays of logic gates.
    * Beyond simple logic gates.
    * Combinational logic word problems
    * Number systems
    * Networks for binary addition
    * Arithmetic logic unit design
    * BCD addition
    * Combinational multiplier
  
  – Labs:
    * LAB 1: Schematic entry and logic simulation using Veribest
    * LAB 2: Logic minimization with espresso
    * LAB 3: Multi-level logic optimization with misII
    * LAB 4: Logic gates, LEDs, and combinational circuit design
  
  – Midterm 1

• Section 2: Sequential logic design (weeks 6-10)
  
  – Lecture topics:
    * Sequential switching networks
    * Timing methodologies
    * Realizing circuits with different kinds of flip-flops
    * Metastability and asynchronous inputs
    * State minimization/reduction
    * State assignment
    * Choice of flip-flops
    * Finite state machine partitioning
    * FSM design with programmable logic
    * FSM design with counters
    * FSM design with more sophisticated programmable logic devices
  
  – Labs:
    * LAB 5: Circuits with feedback: clocks, latches, and counters
    * LAB 6: Basic latch and clocking
    * LAB 7: Registers, RAMs, and Busses
    * LAB 8: Assignment with nova, mustang, and jedi
    * LAB 9: Programmable gate arrays
  
  – Midterm 2
• Section 3: Computer organization and controller design (weeks 11-15)

  – Lecture topics:
    * Structure of a computer
    * Busing strategies
    * FSMs for simple CPUs
    * Random logic
    * Time state (divide and conquer)
    * Jump counter
    * Branch sequencers
    * Microprogramming

  – PROJECT: A 4-bit computer

  – Final - Tuesday May 4th, 7:30-9:30am