Course Information

- Class webpage:
  - www.async.elen.utah.edu/~myers/ec3700
- Get handout #1 for class and contact info.
- Class webpage – see the webpage

TAs and Grader

- Teaching assistants:
  - David Sanderson
  - Jian Zhou
  - James Bergstrom
- Grader
  - Dong-Hoon Yoo
- Lots of office hours, see handout #1.

Discussion Sections

- You must signup for and attend one discussion section.
- Supplemental material given here to help with homework and labs.
- Written assignments will be returned in your discussion section.
- Sections start Wednesday.

Course Description

- Boolean algebra – theory for digital design.
- Overview of implementation technology.
- Combinational logic design.
- Number representations and arithmetic.
- Sequential logic design – sync and async.
- VHDL and CAD tools utilized throughout.

Prerequisites

- Computer programming (CS 2010)
- PHYCS 2220
Textbook


Homework/Labs/Projects

- Homework/lab/project writeups should be turned in to appropriate EE locker.
- Put discussion section number and TA on all assignments.
- Hardware labs checked in discussion section/office hours.
- Homework returned in your discussion section.
- All grading disputes must be made within one week of receiving the grade.

Late Homework/Cheating

- No late homework/labs/projects will be accepted.
- Cheating will be not be tolerated and it will be strongly dealt with. This includes:
  - Passing off someone else’s hardware as yours.
  - Copying someone else’s VHDL code.
  - Copying someone’s homework/exam answers.
  - etc.

Lab Kits

- Many labs will use lab kits.
- These include numerous chips, boards, wires, and design tools.
- Distributed during first discussion section.

Grading Policy

- Homework and Labs – 30 percent
- Midterms – 30 percent
- Project – 20 percent
  - A simple microprocessor
- Final – 20 percent
  - Tuesday, May 1st, 7:00-9:00am

CS/EE 3700 : Fundamentals of Digital System Design

Chris J. Myers
Lecture 1: Design Concepts
Chapter 1
Chip Complexity

• 1963: transistor size = 50µm

• 1975: transistor size = 10µm

• 1985: transistor size = 2µm

• 1995: transistor size = 0.4µm

SIA Roadmap

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Figure 1.1 A silicon wafer
Standard Chips

- Realize common logic functions.
- Usually less than 100 transistors.
- Many common ones found in your lab kits.
- You will use them in a couple of labs.
- Not used much today as they occupy too much space on printed circuit boards (PCB).

Programmable Logic Devices

- They can realize much more complicated logic circuits than a standard chip.
- Often reprogrammable.
- Field-programmable gate arrays (FPGA) will soon use more than 100 million xtors.
- Widely used today.
- You will use in one lab and your project.

Custom-designed Chips

- PLDs are not very efficient so they may not meet performance or cost objectives.
- May need to design a custom or semi-custom chip (also known as an ASIC).
- Advantage: optimized for given task.
- Disadvantage: more complex design and manufacturing process.
- Custom VLSI design taught in CS/EE 5710.

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**Figure 1.2** A field-programmable gate array chip

**Figure 1.3** The development process
Theory and Practice

- Numerous CAD tools available for design.
- Why study the theory and not just the tools?
  - Designer must provide good specification.
  - This theory is utilized in these tools, and it helps you understand what the tools do.
  - Designer must understand the effects of optional processing steps.
  - It is intellectually challenging.