HOMEWORK #2: Logic Design and Implementation

This homework is due at 5pm in the EE locker for CS/EE 3700 on Thursday, January 25, 2001
NO LATE HOMEWORK WILL BE ACCEPTED.

1. Chapter 2, problem 2.5
   Use a Venn diagram to prove:
   \[(x_1 + x_2 + x_3) \cdot (x_1 + x_2 + \overline{x_3}) = x_1 + x_2\]

2. Chapter 2, problem 2.11
   Use algebraic manipulation to find the minimum sum-of-products expression for the function:
   \[f = x_1x_3 + x_1\overline{x_2} + \overline{x_1}x_2x_3 + \overline{x_1}\overline{x_2}x_3\]

3. Chapter 2, problem 2.22
   Design the simplest product-of-sums expression for the function:
   \[f(x_1, x_2, x_3) = \prod M(0, 1, 5, 7)\]

4. Chapter 2, problem 2.30(a)
   Write VHDL code to describe the following functions:
   \[f_1 = x_1\overline{x_3} + x_2\overline{x_3} + \overline{x_3}x_4 + x_1x_2 + x_1x_4\]
   \[f_2 = (x_1 + \overline{x_3}) \cdot (x_1 + x_2 + \overline{x_4}) \cdot (x_2 + \overline{x_3} + \overline{x_4})\]

5. Chapter 3, problem 3.10
   Derive a CMOS complex gate for the logic function:
   \[f(x_1, x_2, x_3, x_4) = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 10)\]

6. Chapter 3, problem 3.36
   Using the style of drawing in Figure 3.66, draw a picture of a PLA programmed to implement
   \[f_1(x_1, x_2, x_3) = \sum m(1, 2, 4, 7).\] The PLA should have the inputs \(x_1, \ldots, x_3\); the product terms \(P_1, \ldots, P_4\); and the outputs \(f_1\) and \(f_2\).

7. Chapter 3, problem 3.44
   Consider the function \(f(x_1, x_2, x_3) = x_1\overline{x_2} + x_1x_3 + x_2\overline{x_3}\). Show a circuit using 5 two-input lookup-tables (LUTs) to implement this expression. As shown in Figure 3.39, give the truth table implemented in each LUT. You do not need to show the wires in the FPGA.

8. Chapter 3, problem 3.55
   What logic gate is realized by the circuit in Figure P3.11? Does this circuit suffer from any major drawbacks?

Note all figures can be found in the lecture notes.