HOMEWORK #2: Communication Channels

This homework is due by midnight on Thursday, September 9, 2004. NO LATE HOMEWORK WILL BE ACCEPTED.

1. Read Chapter 2 and Chapter 3.
2. Complete book problems 2.4.1, 2.4.2, and 2.4.3.
   - Do not use the channel names In and Out which will cause compilation errors. Instead use Inp and Outp.
   - The function send and receive require that the data sent or received must be of type std_logic or std_logic_vector. Therefore, if you which to send a constant, you must do something like this:

```vhd
entity example is
end example;
architecture behavior of example is
signal Ex:channel:=init_channel;
signal Zero:std_logic:='0';
signal One:std_logic:='1';
begnin
env:process
begin
    send(Ex,Zero);
    send(Ex,One);
end process
end behavior;
```
   - You must turn in both the circuit and its environment code.
   - Be sure that your environment code tests your code well enough to convince me that your circuit works.
   - In your turnin, please send all vhd files that you used as well as a README file that gives a one line description of all your files and any instructions for compilation and simulation.
   - Code that does not compile will receive only minimal credit.

3. Complete Problem 2.6.
   - Original source code is available from the course website.
   - Modify the pipelined version of the MiniMIPS.
   - To compile execute.vhd, you will need to not only select 1993 syntax, but also “Use explicit declarations only”.
   - Turn in a modified version of imem.vhd which includes instructions to test your new slt instruction.
   - Turn in any other files which you had to modify to support the new instruction. You do not need to turn in files that you did not modify.

4. Email your VHDL and README files as attachments to (zipped is okay):
   myers@vlisigroup.ece.utah.edu.