Simulation Aided Verification of Analog and Mixed-Signal Circuits

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“...analog has to budget five or six respins. Silicon has become the validation vehicle for analog, and that’s a problem.”
–Sandipan Bhanot, CEO of Knowlent

“If the digital designers did verification the way analog designers do verification, no chip would ever tape out.”
–Sandipan Bhanot, CEO of Knowlent

“...problems are being solved because we have very good analog engineers. But in the future, if we want to improve time-to-market we will have to improve the tools.”
–James Lin, VP at National Semiconductor

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Currently utilizes differential equation (SPICE) simulations.

VHDL/Verilog-AMS only used reluctantly by AMS designers.

High-level models often not accurate or up-to-date.

*Simulation Aided Verification* (SAV) methodology is essential to bridge this gap.

A SAV methodology would allow AMS designers to use their SPICE simulations to create high-level models at right level of abstraction.
Motivating Example: Rambus Ring Oscillator

- A ring oscillator requires an odd number of stages, or does it?
- Jaeha Kim suggested adding bridging circuits to a ring oscillator with an even number of stages.
- Resulting circuit oscillates under a range of transistor sizes.
Rambus Ring Oscillator (Simplified View)
Rambus Ring Oscillator (Detailed View)
Rambus Ring Oscillator Simulation

Ratio of Chain to Bridge Transistors of 0.39

A2
B2

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Rambus Ring Oscillator Simulation

Ratio of Chain to Bridge Transistors of 0.40

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Ratio of Chain to Bridge Transistors of 0.60

Verification of AMS Circuits

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Ratio of Chain to Bridge Transistors of 0.80

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Rambus Ring Oscillator Simulation

Ratio of Chain to Bridge Transistors of 1.20

A2
B2

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Ratio of Chain to Bridge Transistors of 1.60

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Rambus Ring Oscillator Simulation

Ratio of Chain to Bridge Transistors of 2.00

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Ratio of Chain to Bridge Transistors of 2.20
Rambus Ring Oscillator Simulation

Ratio of Chain to Bridge Transistors of 2.25

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Ratio of Chain to Bridge Transistors of 2.275

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Ratio of Chain to Bridge Transistors of 2.30

A2

B2
SAV methodology should be able to construct a model that shows the range of behavior under some variation in parameters.

Marginally functional circuits should fail verification.
LEMA: LHPN Embedded/Mixed-signal Analyzer

- VHDL-AMS Subset
- Safety Property
- Simulation Traces
- Thresholds

Labeled Hybrid Petri Net (LHPN)

- VHDL-AMS Compiler
- Model Generator

- BDD-Based Model Checker
- SMT Bounded Model Checker
- DBM-Based Model Checker

Pass or Fail + Error Trace
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Designers create abstract HDL models manually. Updating these models for circuit changes may be tedious. High quality abstract models require time and expertise. AMS designers typically use detailed transistor level models.
Build abstract models of the circuit using:
- Simulation traces.
- Thresholds on the design variables.
- A property to verify.

1. Assign data to bins
2. Generate rates for binned data
3. Detect discrete multi-valued variables
4. Generate model

- VHDL-AMS Model
- Verilog-AMS Model
- LHPN Model
LHPN for Ratio of 1.60

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### LHPN for Ratio of 2.275

<table>
<thead>
<tr>
<th>Y</th>
<th>1500</th>
<th>1250</th>
<th>900</th>
<th>500</th>
<th>100</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>p34</td>
</tr>
<tr>
<td>p0</td>
<td>p21</td>
<td>p22</td>
<td>p23</td>
<td>p24</td>
<td>p25</td>
<td>p26</td>
</tr>
<tr>
<td></td>
<td>p1</td>
<td>p2</td>
<td>p3</td>
<td>p4</td>
<td>p5</td>
<td>p6</td>
</tr>
<tr>
<td></td>
<td>p0</td>
<td>p11</td>
<td>p14</td>
<td>p7</td>
<td>p8</td>
<td>p9</td>
</tr>
<tr>
<td></td>
<td>p13</td>
<td>p10</td>
<td>p16</td>
<td>p12</td>
<td>p18</td>
<td>p27</td>
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<td>p20</td>
<td>p25</td>
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<td>p15</td>
<td>p28</td>
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<td></td>
<td></td>
<td>p26</td>
<td>p30</td>
<td></td>
<td></td>
<td>p35</td>
</tr>
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<td></td>
<td></td>
<td>p27</td>
<td>p36</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

### Grid

- X-axis: 0, 100, 500, 900, 1300, 1500
- Y-axis: 0, 100, 500, 900, 1250, 1500

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Ring Oscillator Results

- Model generated using simulation results in the middle of the operating region clearly oscillates.
- Model generated using simulation results near the boundary of the operating region includes traces with truncated oscillations.
- Ring oscillator example highlights numerous areas of future work:
  - Selecting a good set of continuous variables, thresholds, and window size can require some effort.
  - Generated model should include trajectories not found in traces.
Future Plans

- Develop a true abstraction-refinement methodology for AMS designs:
  - Refine method for selecting continuous variables and thresholds.
  - Correlated variables should be detected and not modeled.
  - Thresholds should be placed to minimize slew rate ranges.
  - Error traces should be utilized to refine these choices.
- Improve error and coverage metric reporting.
- Adapt or extend property languages for AMS designs.
- Major goal will be to address timing properties.
- Apply these methods to circuits found in flash and other memories.
- Received a new SRC contract to do this research, so looking for new students to work on it.