CE Senior Projects

VLSI Research

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Part One:

Senior Projects
The Engineering Discipline

- **Role**
  - design and build systems
  - change the world around us
    - hopefully for the better...
  - have fun in the process

- **Ultimate requirement**
  - what we build must work!

- **Requisite skills**
  - science: math, physics, chemistry, materials, . . .
  - engineering: circuit design, testing, simulation, programming. . .
  - art: creativity, elegance. . .
  - sociology: team work, presentation skills, technical writing. . .
Computer Engineering

- Design and build computer systems
  - involves both hardware and software design skills
- System software
  - compiler, operating system, device drivers…
  - also interfaces between humans and the hardware
- Hardware
  - analog and digital circuit design
  - board design
  - FPGA design
CE Senior Projects at Utah

- CE program run jointly by ECE and CS departments
- Senior project is capstone of undergraduate program
  - apply what you have learned
  - team based
  - students choose project
  - best method to demonstrate abilities to future employers
- Senior Project is year long activity
  - Next semester: plan and propose project
  - Summer: get parts and start building (optional)
  - Fall of senior year: build and demonstrate
- Student feedback
  - hard, fun, and instructive
  - you get what you put into this
2005 Projects

- Carputer
  - PBDII car data and 802.11g auto-sync to base station
  - monitor our car or your kids

- IR Tag
  - Paintball without the mess

- Athlete monitor system
  - real time tracking of position and heart rate to central coaching station
  - GPS, RT, and Heart Rate Monitor on athlete

- Inverted pendulum 2-wheeled robot

- Multi-carrier reflectometry
  - finding faults in aircraft wires without tearing the plane apart

- Glider avionics package
  - using accelerometers, GPS, and strain sensors
2006 Projects

- PEN
  - electronic paper – the only paper you’ll ever buy!

- Recipedia
  - a cook book that talks and listens to you

- GPS tracker
  - track real time location of campus buses
  - report on cell phone or computer

- OmegaCore
  - a DVR that knows how to remove commercials for you

- NoCPR
  - bathtub drowning prevention

- Tracking Visor
  - virtual reality on your head
Current 2007 Projects

- Wireless positioning measurement system
  - More than just the Wii - use your whole body!
  - Sonar arrays using Zigbee wireless

- Unmanned Autonomous Vehicle
  - Automatic control for a blimp.
  - GPS, wireless

- Aquatic Guidance Systems
  - Look, ma, I can water ski without a driver!

- Hands Free Music Tablet
  - Music scores that change pages for you

- Wi-Fi Clock Radio
  - Wake up to your favorite tunes
Example from 2004

GPS Hummer
Direction and Speed Control

2.2.2.1 H-Bridge schematic
GPS Internals
GPS Parts from Motorola Kit

2.2.6.3 Low Cost Evaluation Kit Contents for the FS Oncore GPS Module

(See Motorola’s Semiconductor Technical Data, Evaluation Tools – Preliminary for the Low Cost Evaluation Kit for the FS Oncore GPS Module)
Autonomous Anti-Collision System

2.2.7.2 Image of the Ultrasonic Range Finder

(See http://www.acroname.com/robotics/parts/R93-SRF04.html)
Completed Car
View of front and Range Finder
GPS Unite connected to $\mu$-Controller
GPS Antenna
Senior Project Synopsys

- This is just a preview
- Diversity in opportunities and problems
- Have fun with the project
  - your chance to do whatever you can dream!
  - if you can imagine it you can usually build it
  - your dedication and time are well rewarded
Part Two:

VLSI
Ubiquitous Nature of VLSI

Ubiquitous

1. existing or being everywhere at the same time
2. constantly encountered

VLSI the process of creating integrated circuits by combining millions of transistors into a single chip.

integrated circuits (IC, silicon chip, microchip, . . . ) miniaturized electronic circuit containing active and passive components which has been manufactured in the surface of a thin substrate of semiconductor material.
transistor A three (or four) terminal solid state semiconductor device that can be used for amplification, switching, voltage stabilization, signal modulation, and many other functions.

- a “switch” is often referred to as a “gate” when abstracted to the mathematical form and used in logic equations.

semiconductor A material with electric conductivity that can both source and sink electrons, and can operate as an insulator and conductor.
Scaling

- Moore’s Law
  - transistor counts double every one to two years
- Cost has followed inverse trend
- Imagine this in other scenarios...
Manufacturing

Size of wafers (single silicon crystal)

200mm/1990 (125/150mm - 1981) → 9 yrs + 2 yrs delay* → 300mm/2001

11 yrs + 0 yrs delay  →  450mm/2012

9 yrs + 0 yrs delay  →  675mm/2019

* 300mm wafer generation delay from 2-year accelerated technology node cycle [return to 3-year cycle (Sc. 2.0) after 2001]
**Proposition:** What you pay for a product is proportional to it’s weight
Part Three:

Research
Learn the rules so you know how to break them properly.

Dalai Lama
Research Cycle

Do

1. learn technology or application
2. build something novel and cool: *a rule breaker!*
3. automate your learnings for productivity

Forever (or until we get alzheimers... )
Why VLSI is Cool

- Artistic and creative pursuit (quite figuratively and literally . . . )
- Satisfaction in doing something new or better
- General satisfaction in products that improve our existence
  - Pentium 4’s all had circuits due to my work!
Circuits and CAD

1. take this simple transistor

2. replicate it $10^8$ times

3. connect instances in ways that break traditional rules

4. write software to support this

Transists and translates into all sorts of fun!
Synopsis of my Research

These are the particular directions I’ve taken VLSI

1. Asynchronous chips and design
2. Relative Timing
3. Transistor and circuit research
4. CAD for VLSI
5. Networks
6. Biological designs
7. Streaming video chips
8. Reliable and Tamper Resistant Circuits
Asynchronous Design

<table>
<thead>
<tr>
<th>Sequencing and timing</th>
<th>Sequencing only</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Traditional clocked design</strong></td>
<td>Not useful</td>
</tr>
<tr>
<td>Pros: Easy to validate, CAD</td>
<td></td>
</tr>
<tr>
<td>Cons: Clock Power</td>
<td></td>
</tr>
<tr>
<td>Best use: homogeneous designs</td>
<td></td>
</tr>
<tr>
<td><strong>Timing ref travels with data</strong></td>
<td><strong>Traditional Async design</strong></td>
</tr>
<tr>
<td>Pros: low latency, power efficient</td>
<td>Pros: Easy to build basic system, robust</td>
</tr>
<tr>
<td>Cons: CAD support</td>
<td>Cons: Slow, power inefficient</td>
</tr>
<tr>
<td>Best use: heterogeneous designs</td>
<td>Best use: designs with high variability</td>
</tr>
</tbody>
</table>

“In the self-timed discipline, sequence and time are connected in the interior of parts called elements.” Mead & Conway, 1980, p218
Asynchronous Design

- 1997 RAPPID Si: 0.25µ, 1.8V, 35°C, for common instr
- Comparing to 400MHz Deschutes Processor

<table>
<thead>
<tr>
<th></th>
<th>RAPPID</th>
<th>Clocked</th>
</tr>
</thead>
<tbody>
<tr>
<td>Throughput [Inst./nS]</td>
<td><img src="chart1" alt="Throughput Bar Chart" /></td>
<td></td>
</tr>
<tr>
<td>Latency [nS]</td>
<td><img src="chart2" alt="Latency Bar Chart" /></td>
<td></td>
</tr>
<tr>
<td>Area [mm²]</td>
<td><img src="chart3" alt="Area Bar Chart" /></td>
<td></td>
</tr>
<tr>
<td>Power [nJ]</td>
<td><img src="chart4" alt="Power Bar Chart" /></td>
<td></td>
</tr>
</tbody>
</table>

Testability: 95.9% (BIST stuck-at)

Key pipeline circuit

Inventing IC design technologies that will be vital to Intel
Learn the Rules: Multiple Input Switching (MIS)

- average pushout of 21% (r00 lib)
- average speedup of 47%
- several sources of effects
- this configuration shows a 28.8% delay pushout

```
G
```

observe effects at this node

```
\begin{align*}
  &a \\
  &b \\
  &c
\end{align*}
```

```
\begin{figure}
  \centering
  \includegraphics[width=\textwidth]{MIS_Pushout.png}
  \caption{MIS Pushout}
  \label{fig:MIS_Pushout}
\end{figure}
```
CAD for automatic MIS vector generation

Cell Name: nand2

Vector Information

- 2 o1+ vects (b a)
  - fh del: 33.56 slp: 30.94
  - hf del: 24.65 slp: 23.13

- 1 o1+ MIS vects (b a)
  - ff del: 15.73 slp: 15.72

- 2 o1- vects (b a)
  - rh del: 20.96 slp: 15.20
  - hr del: 17.65 slp: 16.77

- 1 o1- MIS vects (b a)
  - rr del: 23.55 slp: 16.70

Simulation Results

- o1 r {b f a f} {b:0.47 a:0.64} {b:0.51 a
- o1 f {b r a r} {b:1.12 a:1.33} {b:1.10 a

-E- o1 drives a primary output – completion tree is incomplete

Errors and Warnings
Rule Breaker: Relative Timing (RT)

A huge difference in performance and power is derived by using simple timing assumptions that are easy to represent as a logical constraint and easy to validate in a design.

Speed Independent FIFO Controller (SI)

Relative Timed FIFO Controller (RT-BM)
Apply and Automate: On Chip Networking

Start with your basic $20 \times 20$ mm integrated circuit in a 65nm process.

There are blocks of 100k gates which need to communicate.

Study communication link between pair of logic blocks.
Networking Problem Formulation

- The critical repeater distance of this process is 600 microns (optimal power/performance point)
- This nominal wire will therefore contain $\approx 17$ repeated segments
- Each segment can be flopped
- Bandwidth depends on pipelining

Total distance = 10,000 microns, minimum delay = 30 FO4
Representative Results

10,000$\mu$ 32-bit bus in a 65nm process with low bit activity factor and moderate bus utilization rate:

4-cycle least efficient. Clocked and 2-cycle comparable, source-synchronous better at high frequency.

10,000$\mu$ 32-bit bus in a 65nm process with low bit activity factor and light bus utilization rate:

clocked protocols least efficient. 2-cycle and source-synchronous clearly the best from energy perspective.
Post Office: On Chip Network Implementations

An E-3 Surface

Continuous processing surface.

Each axis passes through each PE exactly once.

Only a single axis of the three are wrapped here for clarity.

Worst case switching diameter = n-1 for an E-n surface.

Sparse population simple - just short the axes.

E-3 surface contains 19 processing elements.
Post Office: On Chip Network Implementation

“The good news is we’ve created a highly sophisticated, multi-function computer that’s the size of a doughnut. The bad news is ... Fitsimmons just dunked it in his cocoa.”
We cannot solve our problems with the same thinking we used when we created them.

Albert Einstein

This is what VLSI is all about.

Let’s think about our problems differently and use this rich canvas to solve them in ways never previously dreamed.