ECE/CS 3720: Embedded System Design  
(ECE 6960/2 and CS 6968)

Chris J. Myers  
Lecture 23: Memory Interfacing

Introduction
- Most embedded systems use only the memory built-in to the microcontroller.
- Memory interfacing and bus timing is important to understanding internal microcontroller architecture.
- Sometimes internal memory is insufficient, and external memory must be used.
- Sometime external devices must be interfaced using memory-mapped I/O.
6811 Expanded Mode

<table>
<thead>
<tr>
<th>Select</th>
<th>R/W</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Write</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Read</td>
</tr>
</tbody>
</table>

Full-Address Decoding
- **Slave** selected only when slave's address is on the bus.
- Design using the following steps:
  1. Write specified address using 0,1,X:
     
     \[0100, 00XX, XXXX, XXXX\] for 1K RAM at $4000-$43FF
  2. Write equation using all 0s and 1s:
     \[select = A_{15} \cdot A_{14} \cdot A_{13} \cdot A_{12} \cdot A_{11} \cdot A_{10}\]

Multiplexed Address and Data Lines

Address Decoder for 1K RAM at $4000-$43FF
Minimal-Cost Address Decoding

- Use don’t cares for unspecified addresses to simplify.

Example:

4K RAM $0000$ to $0FFF$ $0000,XXX,XXX,XXX,XXX$

Input $5000$ $0101,0000,0000,0000$

Output $5001$ $0101,0000,0000,0001$

16K ROM $8000$ to $7FFF$ $11XX,XXX,XXX,XXX,XXX$

Karnaugh Maps

<table>
<thead>
<tr>
<th>Cheaper</th>
<th>Safer</th>
<th>Expandable</th>
</tr>
</thead>
<tbody>
<tr>
<td>A15 A14</td>
<td>A0</td>
<td>A15 A14</td>
</tr>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0 1</td>
<td>0 1</td>
<td>0 1</td>
</tr>
<tr>
<td>1 0</td>
<td>1 0</td>
<td>1 0</td>
</tr>
<tr>
<td>1 1</td>
<td>1 0</td>
<td>1 1</td>
</tr>
</tbody>
</table>
Special Cases

- Size of the memory is not a power of 2.
  - 20K RAM with address range $0000$ to $4$FFF
    - $00XX,XXXX,XXXX,XXXX$ Range $0000$ to $3$FFF
    - $0100,XXXX,XXXX,XXXX$ Range $4000$ to $4$FFF
- Start address divided by memory size not an integer.
  - 32K RAM with address range $2000$ to $9$FFF
    - $001X,XXXX,XXXX,XXXX$ Range $2000$ to $3$FFF
    - $01XX,XXXX,XXXX,XXXX$ Range $4000$ to $7$FFF
    - $100X,XXXX,XXXX,XXXX$ Range $8000$ to $9$FFF

Programmable Address Decoder

Timing Intervals

\[(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + 10\]
\[(\uparrow Y, \downarrow Y) = (\downarrow A, \uparrow A) + [5, 15]\]
\[(\uparrow Y, \downarrow Y) = (\downarrow A + [8, 15], \uparrow A + [5, 12])\]

Available and Required Time Intervals

\[DA = (\downarrow G^* + [10, 20], \uparrow G^* + [0, 15])\]
\[DA = (\downarrow G^* + 20, \uparrow G^*) \text{ worst-case}\]
\[DR = (\uparrow Clk - 30, \uparrow Clk + 5)\]
### Timing Diagrams

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>The input must be valid</td>
<td>The output will be valid</td>
</tr>
<tr>
<td></td>
<td>If the input were to fall</td>
<td>Then the output will fall</td>
</tr>
<tr>
<td></td>
<td>If the input were to rise</td>
<td>Then the output will rise</td>
</tr>
<tr>
<td></td>
<td>Don’t care, it will work regardless</td>
<td>Don’t know, the output value is indeterminate</td>
</tr>
<tr>
<td></td>
<td>Nonsense</td>
<td>High impedance, tristate, HIZ, Not driven, floating</td>
</tr>
</tbody>
</table>

### Read Cycle

#### Read Cycle Circuits

- slave1 data
- slave2 data
- slave3 data

#### Data Bus

- microcomputer

### Write Cycle

#### Write Cycle Circuits

- slave1 data
- slave2 data
- slave3 data

#### Data Bus

- microcomputer
Synchronous Bus Timing

Partially Asynchronous Bus Timing
(6809/680x0/x86)

Fully Asynchronous Read Cycle

Fully Asynchronous Write Cycle
6811 Expanded Mode

- In single chip mode, Port B, Port C, STRA, and STRB are used for I/O.
- In expanded mode:
  - Port B is the high address bits
  - Port C is the low address and data bits
  - STRA is the address strobe AS, and
  - STRB is the R/W line.
General Approach to Memory Interfacing

6811/32K PROM Interface

Read Timing for 32K PROM

6811/32K PROM Interface Timing
### 6811/8K RAM Interface

- **HC138**
- **MCM60L64**
- **A15**
- **A14**
- **A13**
- **R/W**
- **E**
- **B Y3**
- **Select**
- **E+R/W**
- **E1**
- **8K by 8bit**
- **G**, Static RAM
- **W**
- **A12-A8**
- **HC573**
- **LE Q**
- **Port A**
- **A7-A0**
- **DQ7-DQ0**
- **AD7-AD0**

### 6811/8K RAM Interface Write Timing

- **E**
- **R/W**
- **A14-A8**
- **A7-A0**
- **E1**
- **G**
- **W**
- **D7-D0**
- **WDA=(578,533)**
- **WDR=(550,510)**

### Dynamic RAM (DRAM)

<table>
<thead>
<tr>
<th>DRAMs</th>
<th>SRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>High density</td>
<td>Low density</td>
</tr>
<tr>
<td>One xtor, one cap./bit</td>
<td>3-4 xtors/bit</td>
</tr>
<tr>
<td>Slower</td>
<td>Faster</td>
</tr>
<tr>
<td>High fixed cost (refresh)</td>
<td>Low fixed cost (address decoder)</td>
</tr>
<tr>
<td>Low incremental cost</td>
<td>Higher incremental cost</td>
</tr>
<tr>
<td>Address multiplexing</td>
<td>Direct addressing</td>
</tr>
</tbody>
</table>