Lecture 2: I/O Ports

### Fanout Requirements

- **Output when high**
  - $I_{OH}$
  - $I_{IH}$
  - $I_{IL}$

- **Output when low**
  - $I_{OL}$
  - $I_{IH}$
  - $I_{IL}$

### I/O Currents

<table>
<thead>
<tr>
<th>Family</th>
<th>$I_{OH}$</th>
<th>$I_{OL}$</th>
<th>$I_{IH}$</th>
<th>$I_{IL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard TTL</td>
<td>0.4mA</td>
<td>16mA</td>
<td>40μA</td>
<td>1.6mA</td>
</tr>
<tr>
<td>Schottky TTL</td>
<td>1mA</td>
<td>20mA</td>
<td>50μA</td>
<td>2mA</td>
</tr>
<tr>
<td>Low-power Schottky TTL</td>
<td>0.4mA</td>
<td>4mA</td>
<td>20μA</td>
<td>0.4mA</td>
</tr>
<tr>
<td>High-speed CMOS</td>
<td>4mA</td>
<td>4mA</td>
<td>1μA</td>
<td>1μA</td>
</tr>
<tr>
<td>68HC11</td>
<td>0.8mA</td>
<td>1.6mA</td>
<td>1μA</td>
<td>1μA</td>
</tr>
</tbody>
</table>

- fan-out = minimum($I_{OH}/I_{IH}, I_{OL}/I_{IL}$)

### Voltage Thresholds

<table>
<thead>
<tr>
<th>Voltage Levels</th>
<th>5.0V</th>
<th>3.3V</th>
<th>2.5V</th>
<th>1.5V</th>
<th>0.8V</th>
<th>0.4V</th>
<th>0.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$V_OH$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
</tr>
<tr>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
</tr>
<tr>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
</tr>
<tr>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
</tr>
<tr>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
</tr>
<tr>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
<td>$G_{OH}$</td>
</tr>
<tr>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
<td>$G_{IL}$</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
</tr>
<tr>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
<td>$G_{IH}$</td>
</tr>
<tr>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
<td>$G_{OL}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Technology</th>
<th>5V CMOS</th>
<th>3.3V CMOS</th>
<th>2.5V CMOS</th>
<th>1.5V CMOS</th>
<th>0.8V CMOS</th>
<th>0.4V CMOS</th>
<th>0.0V CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
<td>74LS, 74ALS</td>
</tr>
<tr>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
<td>74HC, 74HCT</td>
</tr>
</tbody>
</table>

ECE/CE 3720: Embedded System Design (ECE 6960/2 and CS 6968)

Chris J. Myers
Open-Collector Gates

\[ R \leq \frac{+5 - V_{out}}{I_{out}} \]

Isolated I/O Computer Systems

Memory-Mapped Computer System

Read/Write Cycles
DMA Read/Write Cycles

**DMA Read Cycle**
- **input Devices**: data -> bus
- **Output Devices**: bus -> data

**DMA Write Cycle**
- **input Devices**: data -> bus
- **Output Devices**: bus -> data

**Input Ports**
- **microprocessor**: read from port address
- **Input Port**: read from latch address
- **Q D**: External Control

**Readable Output Port**
- **microprocessor**: read from port address
- **Output Port**: write to port address

**Bidirectional Ports**
- **microprocessor**: read from port address
- **InputOutput Port**: write to port direction register
- **bus**: direction bit
- **D Q**: write to port address
Definitions for I/O Ports
PORTA equ $1000 PA7 i/o, PA6-PA3 outputs, PA2-PA0 inputs
PACTL equ $1026 Bit 7 specifies whether PA7 is i/o
PORTB equ $1004 PB7-PB0 are all readable outputs
PORTC equ $1003 PC7-PC0 can be input or output
DDRC equ $1007 Direction register for Port C
...
#define PORTA *(unsigned char volatile*)(0x1000)
#define PACTL *(unsigned char volatile*)(0x1026)
#define PORTB *(unsigned char volatile*)(0x1004)
#define PORTC *(unsigned char volatile*)(0x1003)
#define DDRC *(unsigned char volatile*)(0x1007)
...

Software to Read Port A and Write Port B
NotGate ldaa PORTA Read from Port A into Reg A
coma Logical complement
staa PORTB Write from Reg A to Port B
bra NotGate

void main(void) { unsigned char data;
while(1) {
    data = PORTA; // Read from Port A
    data = ~data; // Logical complement
    PORTB = data; // Write from Reg A to Port B
}  

Simple I/O Software
clr DDRC Set Port C to input  DDRC = 0x00;
llda PORTC Read Port C into Reg A  H = PORTC;
staa H Store result into memory
llda #$FF Load all 1’s into Reg A  DDRC=0xFF;
staa DDRC Set Port C to output

Init staa DDRC void Init(unsigned char Value) {
    rts DDRC=value; }
Set staa PORTC void Set(unsigned char Value) {
    rts PORTC=value; }
Read ldaa PORTC int Read() {
    rts return(PORTC); }

I/O Example
void init(void){
    DDRC = 0xF0;}// PC7-PC4 outputs, PC3-PC0 inputs
void main(void){
    init(); // call ritual once
    while(1){
        data=PORTC; // input
        data=~data<<4; // complement and shift
        PORTC=data;}} // output
A 4-bit NOT Gate

PORTC equ $1003 ;I/O port
DBRC equ $1007
init ldaa #$F0 ;PC7-PC3 out
staa DBRC ;PC3-PC0 in
rts
org $E000 ;ROM
main lda #XOFF ;SP=$00FF
bsr init ;ritual
loop ldaa PORTC ;input
coma ;logical not
lsla
lsla
lsla
lsla
staa PORTC ;output
bra loop ;repeat
org $FFFE
fdb main ;reset vector