

HOMEWORK #3: Communication Protocols

This homework is due by midnight on Thursday, February 5, 2009.
NO LATE HOMEWORK WILL BE ACCEPTED.

1. Read Chapter 3 and Chapter 4.
2. Perform handshaking expansion on your adder design.
 - **ECE/CS 5750 Students:** Complete book problem 3.5 (i.e., use a bundled data approach).
 - **ECE/CS 6750 Students:** Complete book problem 3.6 (i.e., use a dual-rail approach). For extra credit, use your optimized 1-bit adder design from Problem 2.1.4.
 - Be sure to turn in both the circuit and its environment code.
 - Be sure that your environment code tests your code well enough to convince me that your circuit works.
 - In your turnin, please send all vhd files that you used as well as a README file that gives a one line description of all your files and any instructions for compilation and simulation.
 - Code that does not compile will receive only minimal credit.
 - Email your VHDL and README files as attachments to (zipped is okay):
myers@vlsigroup.ece.utah.edu.
3. Complete Problem 3.13 and turn in either in class or under my door.