

ECE/CS 5750/6750: Asynchronous Circuit Design

Chris J. Myers

Course description

In recent years, there has been a resurgence of interest in the design of asynchronous circuits due to their ability to eliminate clock skew problems, achieve average case performance, adapt to environmental and processing variations, provide component modularity, and lower system power requirements. There is, however, a widely held belief that asynchronous design is difficult and leads to inefficient and unreliable designs. The goal of this course is to dispel this belief by introducing a systematic approach to the design of asynchronous VLSI systems from a high-level specification to an efficient and reliable circuit implementation. This course will include both hands-on experience with existing CAD tools as well as learn the algorithms within them. Topics will include: specification, synthesis, optimization with timing information, performance analysis, and verification.

Prerequisites

Students should have a familiarity with computer programming (CS 2010-2020) and digital logic design (ECE/CS 3700).

Textbook

Asynchronous Circuit Design by Chris J. Myers published by Wiley.

Grading policy

Participation	10 percent
Homework	50 percent
Project	40 percent

Project

A major emphasis of this course will be a final individual project. Students will choose one topic from the course, find research papers on that topic, and implement a computer aided design (CAD) tool. Each student must present the project both in a written report and an oral presentation.

ECE/CS 6750

Students taking ECE/CS 6750 will be expected to solve extra homework problems and complete a more extensive project.

Course Info

COURSE: ECE/CS 5750/6750
Credits: 3
Place: WEB 1230
Time: TTh 10:45am to 12:05pm
Class email: ece6750@vlsigroup.ece.utah.edu
Class webpage: <http://www.async.ece.utah.edu/~myers/ece6750/>

INSTRUCTOR: Chris J. Myers
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Location: MEB 4112
Telephone: 581-6490
Office Hours: TTh 1:00pm - 2:00pm

Syllabus

1. Introduction to asynchronous circuit design
2. Communication channels
 - Modeling asynchronous communication in VHDL
 - Example: MiniMIPS
3. Communication protocols
 - Handshaking expansion
 - Data Encoding
 - Syntax-directed translation
4. Graphical representations
 - Asynchronous finite state machines
 - Petri nets
 - Timed event/level structures
5. Huffman circuits
 - Solving covering problems
 - State minimization
 - State assignment
 - Hazard-free logic synthesis
 - Extensions for MIC operation
6. Muller circuits
 - Complete state coding
 - Hazard-free logic synthesis
 - Hazard-free decomposition
7. Timing circuits
 - Zones
 - POSET Timing
8. Verification
 - Circuit verification
 - Protocol verification
9. Applications
 - History/RAPPID
 - Performance analysis/testing
 - Synchronization problem