Verification of Analog/Mixed-Signal Circuits Using Labeled Hybrid Petri Nets

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System on a chip (SoC) designs are becoming commonplace.
They include digital and analog/mixed-signal (AMS) circuits.
Validation is typically divided since digital requires long time steps while analog requires short time steps.
Strict divisions in SoC validation, however, are rarely possible.
New functional validation methods are needed to support the heterogeneous nature of SoC designs.
Formal verification has shown advantages for digital circuits. Research has begun in formal methods for AMS circuits. AMS verification is complicated by the need to accurately track continuous quantities such as voltages and currents.
Switched Capacitor Integrator Circuit

\[ \frac{dV_{out}}{dt} = \pm 20 \text{ mV/\mu s} \]

\[ \text{freq}(V_{in}) = 5 \text{ kHz} \]

\[ V_{in} = \pm 1000 \text{ mV} \]

\[ C_1 = 1 \text{ pF} \]

\[ C_2 = 25 \text{ pF} \]

\[ \phi_1, \phi_2 \]

\[ \text{freq}(\phi_1) = \text{freq}(\phi_2) = 500 \text{ kHz} \]

\[ dV_{out}/dt = \pm 20 \text{ mV/\mu s} \]
Switched Capacitor Output Waveform

Typical Simulation

![Switched Capacitor Output Waveform](image-url)
Switched Capacitor Integrator Circuit

\[ \frac{dV_{\text{out}}}{dt} = \pm (18 \text{ to } 22) \text{ mV/µs} \]

\[ V_{\text{in}} = \pm 1000 \text{ mV} \]
\[ \text{freq}(V_{\text{in}}) = 5 \text{ kHz} \]
\[ \text{freq}(\Phi_1) = \text{freq}(\Phi_2) = 500 \text{ kHz} \]
\[ C_1 = 1 \text{ pF} \]
\[ C_2 = 25 \text{ pF} \]
Switched Capacitor Integrator Circuit

\[ V_{in} = \pm 1000 \text{ mV} \]
\[ \text{freq}(V_{in}) = 5 \text{ kHz} \]

\[ \text{freq}(\Phi_1) = \text{freq}(\Phi_2) = 500 \text{ kHz} \]
\[ \frac{dV_{out}}{dt} = \pm (18 \text{ to } 22) \text{ mV/\mu s} \]

Does \( V_{out} \) saturate? (i.e. \( -2000 \text{ mV} \geq V_{out} \geq 2000 \text{ mV} \))
Switched Capacitor Output Waveform
Worst Case Simulation

![Graph showing the switched capacitor output waveform with worst-case simulation. The graph plots Vout (mV) against Time (us). The waveform shows a sawtooth pattern with a linearly increasing ramp and periodic oscillations.](image-url)
Crucial to the acceptance of new AMS formal methods is the use of a familiar description language.

The *Labeled hybrid Petri net* (LHPN) model developed to facilitate generation from a VHDL-AMS subset.

We have developed a compiler that generates LHPNs given a circuit description using this subset of VHDL-AMS.
Composed of a Petri net and labels operating on continuous variables and Boolean signals.

Label types are:
- Enablings
- Delay bounds
- Boolean assignments
- Value assignments
- Rate assignments
Labeled Hybrid Petri Nets (LHPNs)

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  - Rate assignments

\[
\begin{align*}
\{l \geq 18\} & \quad [1, 2] \\
\langle \text{max} := T \land \dot{x} := 2 \rangle & \quad [1, 2] \\
\{\text{open}\} & \quad [1, 2] \\
\langle x := 0 \land \dot{x} := -1 \rangle & \quad [1, 2]
\end{align*}
\]
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Labeled Hybrid Petri Nets (LHPNs)

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  - Delay bounds
  - **Boolean assignments**
  - Value assignments
  - Rate assignments
Labeled Hybrid Petri Nets (LHPNs)

- Composed of a Petri net and labels operating on continuous variables and Boolean signals.
- Label types are:
  - Enablings
  - Delay bounds
  - Boolean assignments
  - Value assignments
  - Rate assignments

```
\langle x := 0 \land \dot{x} := -1 \rangle_{[1, 2]}
\langle \text{open} \rangle_{[1, 2]}
\langle \text{max} := T \land \dot{x} := 2 \rangle_{[1, 2]}
\{ l \geq 18 \}
```

```
\langle x := 0 \land \dot{x} := -1 \rangle_{[1, 2]}
\langle \text{open} \rangle_{[1, 2]}
\langle \text{max} := T \land \dot{x} := 2 \rangle_{[1, 2]}
\{ l \geq 18 \}
```
Composed of a Petri net and labels operating on continuous variables and Boolean signals.

Label types are:
- Enablings
- Delay bounds
- Boolean assignments
- Value assignments
- Rate assignments

\[
\begin{align*}
\langle x := 0 \land \dot{x} := -1 \rangle & \quad [1, 2] \\
\{ \text{open} \} & \quad t_1 \\
\langle \text{max} := T \land \dot{x} := 2 \rangle & \quad [1, 2] \\
\{ l \geq 18 \} & \quad t_0 \\
\end{align*}
\]
Piecewise Linear Approximation

\[ mV \]

\[ \mu s \]

- 0
- 50
- 100

- 1800
- 2000
- 2200
Piecewise Linear Approximation

\( mV \)

\( \mu s \)

0

50

100

0

2200

2000

1800

\( 50 \mu s \) to \( 100 \mu s \)
Piecewise Linear Approximation

![Graph of mV vs. µs]

- mV axis labels: 0, 1800, 2000, 2200
- µs axis labels: 0, 50, 100

The graph shows a linear approximation of mV over time (µs).
Piecewise Linear Approximation

The diagram shows a plot with the y-axis labeled $mV$ and the x-axis labeled $\mu s$. The plot includes three linear graphs: one in red, one in blue, and one in purple. The red and blue lines are parallel, while the purple line is steeper. The y-axis ranges from 0 to 2200, with major ticks at 1800 and 2000. The x-axis ranges from 0 to 100, with a major tick at 50. The graphs appear to approximate a piecewise linear function with different slopes in different segments of the x-axis.
architecture behv of integrator is
  quantity Vout,c:real;
  signal inc18:std_logic:=’0’;
  signal inc22:std_logic:=’0’;
  signal clkrst:std_logic:=’0’;
begin
  break Vout=>-1000.0,c=> 0.0;
  c’dot == 1.0;
  break c=> 0.0 when
    clkrst and c’above(100.0);
architecture behv of integrator is
  quantity Vout,c:real;
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architecture behv of integrator is
  quantity Vout,c:real;
signal inc18:std_logic:=’0’;
signal inc22:std_logic:=’0’;
signal clkrst:std_logic:=’0’;
begin
break Vout=>-1000.0,c=> 0.0;
c’dot == 1.0;
break c=> 0.0 when
  clkrst and c’above(100.0);
if inc18='0' use
  if inc22='0' use
    Vout'dot == -22.0;
  else Vout'dot == -18.0;
  end use;
else
  if inc22='0' use
    Vout'dot == 18.0;
  else Vout'dot == 22.0;
  end use;
end use;
If inc18='0' use
  If inc22='0' use
    Vout'dot == -22.0;
  else Vout’dot == -18.0;
  end use;
else
  if inc22='0' use
    Vout’dot == 18.0;
  else Vout’dot == 22.0;
  end use;
end use;

\{inc_{18} \land inc_{22} \land \dot{V}_{\text{out}} \neq -22\} \\
\langle\dot{V}_{\text{out}} := -22\rangle
if inc18='0' use
  if inc22='0' use
    Vout’dot == -22.0;
  else Vout’dot == -18.0;
  end use;
else
  if inc22='0' use
    Vout’dot == 18.0;
  else Vout’dot == 22.0;
  end use;
end use;
process begin
  assign(inc18,'1',0,0);
  assign(inc22,'1',0,100);
  wait until c'above(100.0);
  assign(clkrst,'1',0,0);
  wait until not c'above(100.0);
  assign(clkrst,'0',0,0);
  assign(inc18,'0',0,0);
  assign(inc22,'0',0,100);
  wait until c'above(100.0);
  assign(clkrst,'1',0,0);
  wait until not c'above(100.0);
  assign(clkrst,'0',0,0);
end process;
process begin
assign(inc18,'1',0,0);
assign(inc22,'1',0,100);
wait until c'above(100.0);
assign(clkrst,'1',0,0);
wait until not c'above(100.0);
assign(clkrst,'0',0,0);
assign(inc18,'0',0,0);
assign(inc22,'0',0,100);
wait until c'above(100.0);
assign(clkrst,'1',0,0);
wait until not c'above(100.0);
assign(clkrst,'0',0,0);
end process;
process begin
  assign(inc18, '1', 0, 0);
  assign(inc22, '1', 0, 100);
  wait until c'above(100.0);
  assign(clkrst, '1', 0, 0);
  wait until not c'above(100.0);
  assign(clkrst, '0', 0, 0);
  assign(inc18, '0', 0, 0);
  assign(inc22, '0', 0, 100);
  wait until c'above(100.0);
  assign(clkrst, '1', 0, 0);
  wait until not c'above(100.0);
  assign(clkrst, '0', 0, 0);
end process;
process begin
  assign(inc18,'1',0,0);
  assign(inc22,'1',0,100);
  wait until c'above(100.0);
  assign(clkrst,'1',0,0);
  wait until not c'above(100.0);
  assign(clkrst,'0',0,0);
  assign(inc22,'0',0,100);
  wait until c'above(100.0);
  assign(clkrst,'1',0,0);
end process;
Finding all reachable states of the system is necessary to verify properties about the system.

LHPNs are infinite state systems.

Reachability analysis must represent this infinite state space using finite state equivalence classes.
Finite State Representation

Hartong, et al.

Little, et al.

Frehse, Gupta, Krogh, Rutenbar
Zones

- Only allow polygons with $45^\circ$ and $90^\circ$ angles.
- Evolve at a rate of 1 along $45^\circ$ angles.
- Use variable substitutions to support other rates.
- Warping used to ensure $45^\circ$ and $90^\circ$ angles are maintained.
Warping the Zone

\[ \begin{align*}
0 \leq x &\leq 3 \\
1 \leq y &\leq 4 \\
x - y &\leq 2 \\
y - x &\leq 4
\end{align*} \]

\[
\begin{cases}
\dot{x} := 2 \\
\dot{y} := 3
\end{cases}
\]

\[
[2, 5] \quad t_0
\]

\[
p_0
\]
Warping the Zone

\[ 2 \leq x \leq 8 \]
\[ 3 \leq y \leq 9 \]
\[ x - y \leq 2 \]
\[ y - x \leq 4 \]

\( \hat{x} := 2 \)
\( \hat{y} := 3 \)

\[ p_0 \]

\[ t_0 \]

\[ [2, 5] \]
Warping the Zone

\begin{align*}
  1 & \leq 2x \leq 4 \\
  1 & \leq 3y \leq 3 \\
  2x - 3y & \leq \frac{2}{3} \\
  3y - 2x & \leq \frac{4}{3}
\end{align*}

\[ \langle \dot{x} := 2 \rangle \]

\[ \langle \dot{y} := 3 \rangle \]
Warping the Zone

\[\begin{align*}
1 & \leq 2x \leq 4 \\
1 & \leq 3y \leq 3 \\
2x - 3y & \leq 2 \\
3y - 2x & \leq 1
\end{align*}\]
Warping the Zone

\[
\begin{align*}
1 & \leq 2x \leq 4 \\
1 & \leq 3y \leq 3 \\
2x - 3y & \leq 2 \\
3y - 2x & \leq 1
\end{align*}
\]

\[
\langle \dot{x} := 2 \rangle \\
\langle \dot{y} := 3 \rangle
\]

\[
[2, 5] \\
p_0 \\
t_0
\]
assert vout’above(-2000) and
not vout’above(2000)
report "Integrator saturates"
severity failure;

\[
\begin{align*}
\{ V_{out} \leq -2000 \text{V} \\
V_{out} \geq 2000 \}
\end{align*}
\langle fail := T \rangle
Switched Capacitor Integrator Example

\[
\dot{V}_{\text{out}} = -18
\]

\[
\{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq -22 \}
\{ \dot{V}_{\text{out}} := -22 \}
\]

\[
\{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq -18 \}
\{ \dot{V}_{\text{out}} := -18 \}
\]

\[
\{ \text{inc18} \land \lnot \text{inc22} \land \dot{V}_{\text{out}} \neq -22 \}
\{ \dot{V}_{\text{out}} := -22 \}
\]

\[
\{ \text{inc18} \land \lnot \text{inc22} \land \dot{V}_{\text{out}} \neq -18 \}
\{ \dot{V}_{\text{out}} := -18 \}
\]

\[
\{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq 18 \}
\{ \dot{V}_{\text{out}} := 18 \}
\]

\[
\{ \text{inc18} \land \lnot \text{inc22} \land \dot{V}_{\text{out}} \neq 18 \}
\{ \dot{V}_{\text{out}} := 18 \}
\]

\[
\left\{ \begin{array}{l}
\text{c} \geq 100 \land \lnot \text{fail} \\
\text{clkrst} := T
\end{array} \right. \\
\{ \dot{V}_{\text{out}} \leq -2000 \lor \dot{V}_{\text{out}} \geq 2000 \}
\]

\[
\{ \text{fail} := T \}
\{ \text{c} := 0 \mu s \}
\]
Switched Capacitor Integrator Example

\[ c = 0\mu s \]

\[ V_{out} = -1000mV \]

\( inc18 = T, inc22 = F \ clkrst = F, fail = F \)
Switched Capacitor Integrator Example

\[ \text{Switched Capacitor Integrator Example} \]

\[ t_2 \quad \{ \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq 22 \} \quad \langle V_{\text{out}} := 22 \rangle \]

\[ t_1 \quad \{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq 22 \} \quad \langle V_{\text{out}} := -22 \rangle \]

\[ t_3 \quad \{ \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq 18 \} \quad \langle V_{\text{out}} := -18 \rangle \]

\[ t_4 \quad \{ \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq -22 \} \quad \langle V_{\text{out}} := -22 \rangle \]

\[ t_5 \quad \{ \text{fail} \} \quad \langle \text{clkrst} := T \rangle \]

\[ t_6 \quad [0, 100] \quad \{ \text{fail} \} \quad \langle \text{inc22} := T \rangle \]

\[ t_7 \quad \{ \text{c} \geq 100 \land \text{fail} \} \quad \langle \text{clkrst} := F \rangle \]

\[ t_8 \quad \{ \text{c} \geq 100 \land \text{fail} \} \quad \langle \text{clkrst} := F \rangle \]

\[ t_9 \quad \{ \text{fail} \} \quad \langle \text{inc18} := F \rangle \]

\[ t_{10} \quad \{ \text{fail} \} \quad \langle \text{inc22} := F \rangle \]

\[ t_{11} \quad \{ \text{c} \geq 100 \land \text{fail} \} \quad \langle \text{clkrst} := T \rangle \]

\[ t_{12} \quad \{ \text{fail} \} \quad \langle \text{inc18} := T \rangle \]

\[ t_{13} \quad \{ V_{\text{out}} \leq -2000 \lor V_{\text{out}} \geq 2000 \} \quad \langle \text{fail} := T \rangle \]

\[ \{ \text{clkrst} \land \text{c} \geq 100 \} \quad \langle \text{c} := 0 \rangle \]

\[ 0 \mu s \leq \text{c} \leq 100 \mu s \]

\[ -1000 \text{mV} \leq V_{\text{out}} \leq 800 \text{mV} \]

\[ \text{inc18} = T, \text{inc22} = F \quad \text{clkrst} = F, \text{fail} = F \]
Switched Capacitor Integrator Example

\[ \begin{align*}
\{ & \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq 22 \} \\
V_{\text{out}} := 22 \end{align*} \]

\[ \begin{align*}
\{ & \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq 22 \} \\
\dot{V}_{\text{out}} := 22 \end{align*} \]

\[ \begin{align*}
\{ & \text{inc18} \land \text{inc22} \land V_{\text{out}} \neq 18 \} \\
V_{\text{out}} := 18 \end{align*} \]

\[ \begin{align*}
\{ & \text{c} \geq 100 \land \text{fail} \} \\
\text{inc18} := T \end{align*} \]

\[ \begin{align*}
\{ & \text{c} \geq 100 \land \text{fail} \} \\
\text{inc18} := F \end{align*} \]

\[ \begin{align*}
\{ & \text{c} \geq 100 \land \text{fail} \} \\
\text{clkrst} := T \end{align*} \]

\[ \begin{align*}
\{ & \text{c} \geq 100 \land \text{fail} \} \\
\text{clkrst} := F \end{align*} \]

\[ \begin{align*}
\{ & \text{fail} \} \\
\text{inc18} := T \end{align*} \]

\[ \begin{align*}
\{ & \text{fail} \} \\
\text{inc18} := F \end{align*} \]

\[ \begin{align*}
\{ & \text{V}_{\text{out}} \leq -2000 \lor V_{\text{out}} \geq 2000 \} \\
\text{fail} := T \end{align*} \]

\[ \begin{align*}
\{ & \text{clkrst} \land \text{c} \geq 100 \} \\
\text{c} := 0 \end{align*} \]

0μs ≤ c ≤ 100μs

-1000mV ≤ V_{out} ≤ 800mV

inc18 = T, inc22 = T clkrst = F, fail = F
Switched Capacitor Integrator Example

\[
\begin{align*}
&{\{inc18 \land inc22 \land } \\
&\dot{V}_{out} \neq 22\} \\
&\langle V_{out} := 22 \rangle \\
&{\{inc18 \land inc22 \land } \\
&\dot{V}_{out} \neq -22\} \\
&\langle V_{out} := -22 \rangle \\
&{\{inc18 \land \neg inc22 \land } \\
&\dot{V}_{out} \neq 18\} \\
&\langle V_{out} := 18 \rangle \\
&\{\neg inc18 \land inc22 \land } \\
&\dot{V}_{out} \neq -18\} \\
&\langle V_{out} := -18 \rangle
\end{align*}
\]

\[
\begin{align*}
0 \mu s & \leq c \leq 100 \mu s \\
-1000 mV & \leq V_{out} \leq 1200 mV \\
inc18 & = T, inc22 = T \quad clkrst = F, fail = F
\end{align*}
\]
Switched Capacitor Integrator Example

\[
\{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq -22 \} \\
\{ \text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq 18 \}
\]

\[
\{ \text{c} \geq 100 \land \text{fail} \}
\]

\[
\{ \text{inc18} := T \}
\]

\[
\{ \text{inc22} := T \}
\]

\[
\{ \text{inc18} := F \}
\]

\[
\{ \text{inc22} := F \}
\]

\[
\{ \text{c} \geq 100 \land \text{fail} \}
\]

\[
\{ \text{clkrst} := T \}
\]

\[
\{ \text{clkrst} := F \}
\]

\[
\{ \text{inc18} := T \}
\]

\[
\{ \text{fail} := T \}
\]

\[
\{ \text{fail} := F \}
\]

\[
\{ \text{c} \geq 100 \land \text{fail} \}
\]

\[
\{ \text{V}_{\text{out}} \leq -2000 \lor \text{V}_{\text{out}} \geq 2000 \}
\]

\[
\{ \text{clkrst} \land \text{c} \geq 100 \}
\]

\[
\{ \text{c} := 0 \}
\]

\[
800\,\text{mV} \leq \text{V}_{\text{out}} \leq 1200\,\text{mV}
\]

\[
\text{inc18} = T, \text{inc22} = T, \text{clkrst} = T, \text{fail} = F
\]
Switched Capacitor Integrator Example

\[ \text{c} = 0 \mu s \]

\[ 800 \text{mV} \leq V_{\text{out}} \leq 1200 \text{mV} \]

inc18 = T, inc22 = T clkrst = T, fail = F
\[
\begin{align*}
  &c = 0 \mu s \\
  &800 mV \leq V_{out} \leq 1200 mV \\
  &inc18 = T, \ inc22 = T \ clkrst = F, \ fail = F
\end{align*}
\]
Switched Capacitor Integrator Example

\[\text{inc18} \land \text{inc22} \land \dot{V}_{\text{out}} \neq 22\]
\[\dot{V}_{\text{out}} := \text{22}\]
\[\langle \text{inc18} := \text{T} \rangle\]
\[\text{c} \geq 100 \land \overline{\text{fail}}\]
\[\langle \text{clkrst} := \text{F} \rangle\]
\[\text{fail} \]
\[\langle \text{inc18} := \text{F} \rangle\]

\[c = 0 \mu\text{s}\]

\[400 \text{mV} \leq V_{\text{out}} \leq 1600 \text{mV}\]

\[\text{inc18} = \text{T}, \text{inc22} = \text{T} \quad \text{clkrst} = \text{F}, \text{fail} = \text{F}\]
Switched Capacitor Integrator Example

\[ c = 0 \mu s \]

\[ 0 mV \leq V_{out} \leq 2000 mV \]

\[ inc18 = T, \ inc22 = T \quad \text{clkrst} = F, \ fail = F \]
Switched Capacitor Integrator Example

\[ c = 0 \mu s \]

\[ 0 \text{mV} \leq V_{out} \leq 2000 \text{mV} \]

\[ inc18 = T, \quad inc22 = T \quad clkrst = F, \quad fail = T \]
Corrected Switched Capacitor Integrator

\[ V_{\text{in}} = \pm 1V \]
\[ \text{freq}(V_{\text{in}}) = 5 \text{ kHz} \]

\[ V_{\text{out}} = 22 \text{ to } 24 \text{mV/} \mu \text{s when } V_{\text{out}} \leq -1000 \]
\[ 16 \text{ to } 22 \text{mV/} \mu \text{s when } V_{\text{out}} > -1000 \]
\[ -(22 \text{ to } 24) \text{mV/} \mu \text{s when } V_{\text{out}} > 1000 \]
\[ -(16 \text{ to } 22) \text{mV/} \mu \text{s when } V_{\text{out}} \leq 1000 \]
## Verification Results

<table>
<thead>
<tr>
<th>Example</th>
<th>LHPN Method</th>
<th>HPN</th>
<th>HYTech</th>
<th>PHAVer</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Time</td>
<td>Verifies?</td>
<td></td>
</tr>
<tr>
<td>Int. (Sat.)</td>
<td>103</td>
<td>0.24</td>
<td>No</td>
<td>143</td>
</tr>
<tr>
<td>Int. (Unsat.)</td>
<td>142</td>
<td>0.23</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>Diode (Osc.)</td>
<td>115</td>
<td>0.84</td>
<td>Yes</td>
<td>2321</td>
</tr>
<tr>
<td>Diode (Nonosc.)</td>
<td>132</td>
<td>1.20</td>
<td>No</td>
<td>2529</td>
</tr>
</tbody>
</table>

- **Example**: The examples shown include 'Int. (Sat.)', 'Int. (Unsat.)', 'Diode (Osc.)', and 'Diode (Nonosc.)'.
- **LHPN Method**: The leftmost column lists the examples.
- **Time**: The time taken for verification.
- **Verifies?**: Whether the method verifies the example.
- **HPN**: The verification results for HPN.
- **HYTech**: The verification results for HYTech.
- **PHAVer**: The verification results for PHAVer.

### Circuit Diagram

```
  V_{in}  \quad R \quad L \quad I_{1} \quad C \quad V_{c}
```

- **Symbol**: The symbols represent electronic components: $V_{in}$ (input voltage), $R$ (resistor), $L$ (inductor), $I_{1}$ (current source), $C$ (capacitor), and $V_{c}$ (voltage output).
- **Connections**: The circuit is connected in a feedback configuration with an input voltage $V_{in}$, a resistor $R$, an inductor $L$, a current source $I_{1}$, a capacitor $C$, and an output voltage $V_{c}$.
Conclusions

- LHPN model is used to describe and analyze AMS circuits.
- VHDL-AMS code can be translated to an LHPN.
- Reachability algorithms developed to support LHPNs.
- Preliminary results are encouraging.
Future Work

- Create a SPICE deck compiler for LHPNs.
- Develop methods to improve user feedback when a failure is detected or provide coverage metrics when no failure is found.
- Develop complete system LHPN models that include both analog and digital hardware as well as embedded software.