Research Statement

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Prior and Current Research

Timed Circuit Verification

During my undergraduate education, I participated in several projects related to asynchronous design, timed circuit verification, and testing. For my senior thesis, I implemented a timing verification algorithm using future variables in the ATACS tool and compared the results of this new algorithm to previously implemented past variable algorithms. The work concluded that future variables are a superior approach, but partial order reductions should be applied selectively.

Hybrid Systems Validation

Due to increasing design complexity and process variation the validation problem for analog/mixed-signal circuits is an increasing concern for industrial design teams (Chang, 2007). My dissertation work explores the modeling and formal verification of hybrid systems with emphasis on analog/mixed-signal circuits as the motivating examples for the work. We have developed novel methods for automatic model generation from a set of simulation traces of the system. The model generation system produces labeled hybrid Petri nets, Verilog-AMS, and VHDL-AMS. These automatically generated models are used for automatic verification of desired system properties. The verification method finds the reachable state space of the hybrid model. This state space exploration is complicated by the need to represent continuously varying quantities. To increase the efficiency of the state space exploration my algorithm uses a restricted form of convex polyhedra to conservatively represent the state space. This work promises to find complex bugs not easily exposed by a simulation-only methodology. Furthermore, automatic abstract model generation can produce abstract models suitable for system-level simulation that perform up to 40x faster.

Future Research Plan

Analog/Mixed-Signal Circuit Validation

The simulation-only validation methodology primarily used today in analog/mixed-signal circuit validation is not adequate for the increasing complexity of analog/mixed-signal designs. In fact, functional failures are now becoming more pronounced than performance failures for complex mixed-signal designs. Simulation only methodologies provide a poor solution to combat this problem. My long term research goal is to provide a practical, formalized methodology and tools for the validation of large mixed-signal systems fabricated on modern processes. This methodology will provide a mix of semi-formal and formal methods that enable engineers to design and validate large mixed-signal circuits on increasingly variable processes. Initially, I plan to address automatic stability verification, automatic model abstraction, AMS circuit monitors, and an AMS property specification language.

- **Automatic Stability Verification**
  Stability is a critical property of many difficult to design analog circuits such as PLLs and oscillators. Automatically determining the stable points of a transistor-level circuit over a range of parameters would greatly aid the validation process of these circuits. Previous work in this direction has yielded interesting but impractical results. I believe that combining previous work with abstract modeling methods can produce a viable solution.
- **Automatic Model Abstraction**
  The increasing complexity of mixed-signal designs is putting a strain on the simulation dependent validation methodology. To enable more system-level simulations automatic methods are needed for abstract model generation. There has been significant work in abstract modeling of analog circuits. I plan to extend this work by improving the efficiency of the methods, developing methods to quantify model quality, and enabling the use of these abstract models by formal verification tools.
- **AMS Circuit Monitors**
  Semi-formal methods show strong promise for analog/mixed-signal circuits due to the computational complexity of formal methods. Run-time verification of simulation traces using property based monitors is one of these promising semi-formal techniques. Initial exploration into this area using

the tool AMT shows promise (Nickovic, 2007). Further work in online verification methods and automatic property extraction are necessary.

- **AMS Property Language**

  A formal property specification language is necessary for designers to describe properties of the system. There are several property specification languages in use for digital systems such as PSL, SVA, etc. These languages are inadequate for specifying properties of analog/mixed-signal circuits. Several groups have proposed their own property specification languages. These languages all have their shortcoming in expressiveness or ease of use. I plan to work with analog designers to design a property specification language that meets their needs.

Embedded Systems Validation

Embedded systems are mixed domain systems where improved validation methods are needed due to the complex interactions between hardware and software. There is a growing body of work in software verification that can be combined with the growing body of work in mixed-signal circuit verification to provide a comprehensive verification solution for embedded systems. My long term research goal is to provide a set of tools that enable automated embedded system validation. I will begin working on hardware/software modeling and co-verification and embedded software verification.

- **Hardware/Software Modeling and Co-verification**

  Validation of embedded systems is complicated by the mix of software and hardware. Many current approaches to embedded systems verification fail to model the system with adequate detail. To verify the critical properties of embedded systems, it is necessary to model the software at the assembly level and the hardware as an analog/mixed-signal system. Modeling at this level of detail can be accomplished with extensions to labeled hybrid Petri nets (LHPNs). Verification methods on this class of extended LHPNs can be derived from algorithms developed in my dissertation.

- **Embedded Software Verification**

  There is a growing body of work in software verification of languages like C or Java. This work can be leveraged and adapted to the unique features of embedded software. While many interesting properties can be verified on high level languages, many properties of embedded systems must be verified at the assembly level while taking into account events like hardware interrupts. Extensions to current software verification methodologies to function at the assembly level and include additional details like interrupt requirements are necessary.

Concurrent Systems Validation

In the world of multi-core microprocessor systems and parallel programs, concurrent systems validation is becoming increasingly important. Correctly reasoning about concurrent systems is difficult if not impossible for engineers and designers. Providing the tools necessary to enable the correct and efficient design of concurrent hardware and software systems is my goal.

- **Multi-core Hardware Verification:**

  Verifying digital hardware systems is a mature discipline. With the growing popularity of multi-core systems new problems and complexities have become apparent. In a single core system, replaying an error trace in a deterministic manner is straightforward. This is not the case with multi-core systems. Clever run-time techniques to capture and potentially diagnose concurrency related bugs would prove very useful. As the number of cores increase, the model complexity also grows dramatically. Abstraction techniques to deal with the unique characteristics and model complexity of multi-core systems are a compelling research problem.

- **Parallel Software Verification**

  The increased interest in novel parallel programming techniques presents an opportunity to integrate formal specifications and development methods into the software engineering culture. For instance, libraries to support parallel programming are being created and used. Developing mechanisms to ensure or prove correctness of these new libraries provides tremendous benefit to the users of these libraries.

Collaboration

Industry

Through my interactions with the Semiconductor Research Corporation and internships I have developed good working relationships with Cadence, Freescale, and Rambus. These interactions have provided valuable feedback in addition to funding opportunities for my research. I intend to continue and strengthen these interactions. I also intend to build new relationships as appropriate through networking and my student's internships.

Academia

My research provides many opportunities for collaboration between disciplines including researchers in: analog circuit design, computer aided design, controls, embedded systems, formal methods, mathematics, and software engineering. I have had several opportunities to collaborate with other disciplines as a graduate student. I plan to continue many of these collaborations as well as form new collaborations as my research develops and diversifies.

Students

Students are the key to any successful research program. I plan to incorporate and develop the fresh ideas and innovation of students at all levels into my research program. I had the opportunity to be involved in a research group as a freshman. In addition to my own experiences, I have seen and helped mentor several other undergraduate students in our lab. I feel that undergraduates are a valuable addition to a research lab as they learn what graduate students do and how research works in addition to providing graduate students opportunities to help in the mentoring of younger researchers, an invaluable skill as they move forward in their careers. I plan to have a dynamic research group including both graduate and undergraduate students.