Figure 15: Timed implementation of the DRAM controller.

Figure 16: Complex-gate implementation of cas signal for the DRAM controller.
All unmarked solid rules have timing constraint \([0,2]\).
All dashed rules have timing constraint \([0,0]\).

Figure 13: Well-formed Constraint graph specification for the \textit{refresh} cycle of the DRAM controller.

Figure 14: Removal of data dependence from the DRAM controller specification.
Figure 11: Burst-mode specification for the DRAM controller (courtesy of [13]).

Figure 12: Constraint graph specification for the refresh cycle of the DRAM controller.
Figure 9: (a) Speed-independent implementation of the MMU controller. (b) Timed implementation of the MMU controller.

Figure 10: Block diagram for the DRAM controller (courtesy of [13]).
Figure 7: The cyclic constraint graph specification for the optimized MMU.

Figure 8: The cyclic constraint graph specification for the persistent MMU.
Figure 5: Block diagram for part of the MMU controller.

Figure 6: The cyclic constraint graph specification for the unoptimized MMU.
Figure 3: (a) State graph for the SCSI protocol controller.
(b) Reduced state graph for the SCSI protocol controller.

\[
\begin{align*}
\neg \text{ack} & \quad \neg \text{rdy} \quad + \quad \text{gC} \quad \text{req} \\
\neg \text{q} & \\
\neg \text{ack} \land \neg \text{rdy} \land \neg \text{q} & \rightarrow \text{req}^\uparrow \\
\text{ack} \land \text{q} & \rightarrow \text{req}^\downarrow \\
\end{align*}
\]

Figure 4: (a) Speed-independent implementation of \( \text{req} \).
(b) Timed implementation of \( \text{req} \).
Figure 1: The cyclic constraint graph for a SCSI protocol controller (courtesy of [20]).

Figure 2: A subgraph of the infinite acyclic constraint graph for the SCSI protocol controller.